No. 14-1569

IN THE

United States Court of Appeals for the Federal Circuit

SYNTEST TECHNOLOGIES, INC.,

Plaintiff-Appellant,

v.

CISCO SYSTEMS, INC.,

Defendant-Respondent.

ON APPEAL FROM THE UNITED STATES DISTRICT COURT FOR THE NORTHERN DISTRICT OF CALIFORNIA, CASE NO. 5:12-CV-05965, HON. PAUL S. GREWAL

BRIEF OF APPELLANT

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August 22, 2014

CERTIFICATE OF INTEREST

Pursuant to Federal Circuit Rule 47.4, counsel of record for Plaintiff-Appellant certifies as follows:

1) The full name of every party represented by us is SynTest Technologies, Inc.

2) The names of the real parties in interest represented by us are: Not applicable.

3) All parent corporations and any publicly held companies that own 10% or more of the stock of the parties represented by us: None.

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STATEMENT OF RELATED CASES

Pursuant to Rule 47.5 of the Federal Circuit Rules of Appellate Procedure, there are no other appeals in or from this civil action that were previously before this or any other appellate court.

JURISDICTIONAL STATEMENT

Plaintiff-Appellant SynTest Technologies, Inc. ("SynTest") takes this appeal from the judgment entered by the Honorable Paul S. Grewal on June 12, 2014, in favor of Defendant-Respondent Cisco Systems, Inc. ("Cisco"). A1. The notice of appeal was timely filed on June 17, 2014. A1414. Pursuant to 28 U.S.C. § 1295(1)(a), this Court has jurisdiction over the judgment that Cisco does not infringe U.S. Patents Nos. 7,006,213 ("the '213 patent"), 7,434,126 ("the '126 patent") and 7,779,323 ("the '323 patent") (collectively "the patents-in-suit"). *Aventis Pharmaceuticals v. Amino Chemicals Ltd*., 715 F.3d 1363, 1372 (Fed. Cir. 2013) (recognizing this Court's jurisdiction over a stipulated judgment following a claim construction ruling that rendered the accused instrumentality non-infringing).

STATEMENT OF ISSUES

1) Did the District Court err in limiting the ways of "applying an ordered sequence of capture clocks" to automatic "triggering" of the capture clocks?

2) Did the District Court err in limiting "each shift clock pulse" to a clock "pulse of the capture clock"?

3) Did the District Court err in limiting "capture clock" to a "reconfigured system clock"?

STATEMENT OF THE CASE

I. THE TECHNOLOGY

The invention claimed by the patents-in-suit "generally relates to the testing of logic designs in an integrated circuit . . . embedded with design-for-test (DFT) techniques." A139 at 1:12-15. "[A] primary objective of the present invention is to provide an improved multiple-capture DFT system implementing the multiple-capture DFT technique." A140 at 3:38-41. This improved "multiple-capture DFT system . . . comprises applying an ordered sequence of capture clocks and operating each capture clock at its selected clock speed in the capture operation (cycle)." A141 at 5:33-37.

A. Integrated Circuits or ASICs

Understanding the operation of relevant integrated circuits – known as application-specific integrated circuits ("ASICs") – informs how they are tested. ASICs can contain billions of transistors or storage elements. A1179-1180. In use, ASICs receive instructions to place some or all of their storage elements in a particular state – 1 or 0 – and based on the instructed state, provide an output.

A1189. This process of generating an output based only on an input received is referred to as combinational logic. A61, A565 at 1:14-19.

An ASIC's tasks must be broken down into steps, and the timing of the steps is sequenced by an electric signal – typically a square wave – which is referred to as a clock signal or simply as a clock. A56, A1190. A clock signal's frequency – often referred to as clock speed – is expressed in hertz. A57, A1193. The higher the frequency, the faster each new input is received and output is provided; *i.e.*, the faster each step is performed. Stated simply, each step corresponds to a cycle of the square wave, which is commonly referred to as a clock pulse. A56. Today's ASICs can operate at frequencies exceeding a gigahertz. A330, A537 at 1:27-29.

Clocks are distinct from the mechanisms for generating the signal. A1193, 1131 at 7:3-18. In summary, a clock refers to the signal itself, a clock pulse is one cycle of the signal, clock speed refers to the frequency of the cycles, and clock source refers to the mechanism generating the signal. A1193.

ASICs can simultaneously perform multiple tasks. During normal operations, different portions or regions of a circuit can be controlled by different clocks. A139 at 1:32-39, A1131 at 8:5-16, A1194. Such regions are referred to as clock domains. *Id*. The same domain can at different times be controlled by different clocks. *Id*. A different clock means a clock signal from a different source or from the same source, but with a different frequency. *Id.* A particular domain's

system clock refers to the timing signal from a particular source and at a particular frequency that typically controls the domain during normal operation. *Id.*

Through manipulation – multiplication, division or suppression – the same clock source can generate different system clocks serving different domains. A1195. One clock source can simultaneously provide multiple clocks at different speeds to different domains. A1195, A139 at 1:36-39. Alternatively, different clock domains can be controlled by system clocks generated from different sources. A1194, A139 at 1:33-39. The tasks performed by an ASIC can require different domains controlled by different system clocks to interact with each other. A330.

B. Testing of ASICs

At a basic level, an ASIC depends on the state of its storage elements, sometimes referred to as flip flops. A330. ASIC testing, therefore, includes testing to ensure that a flip flop is not stuck in a state – referred to as a stuck-at fault – and to ensure that the flip flop can complete a state transition before receiving its next instruction – referred to as a delay fault. A1189-91.

The scan technique is a common method for testing ASICs. A589. It involves modifying each flip flop to allow for the sequential input of known data – a known state of the flip flop – into a series of flip flops, which for scan-test are

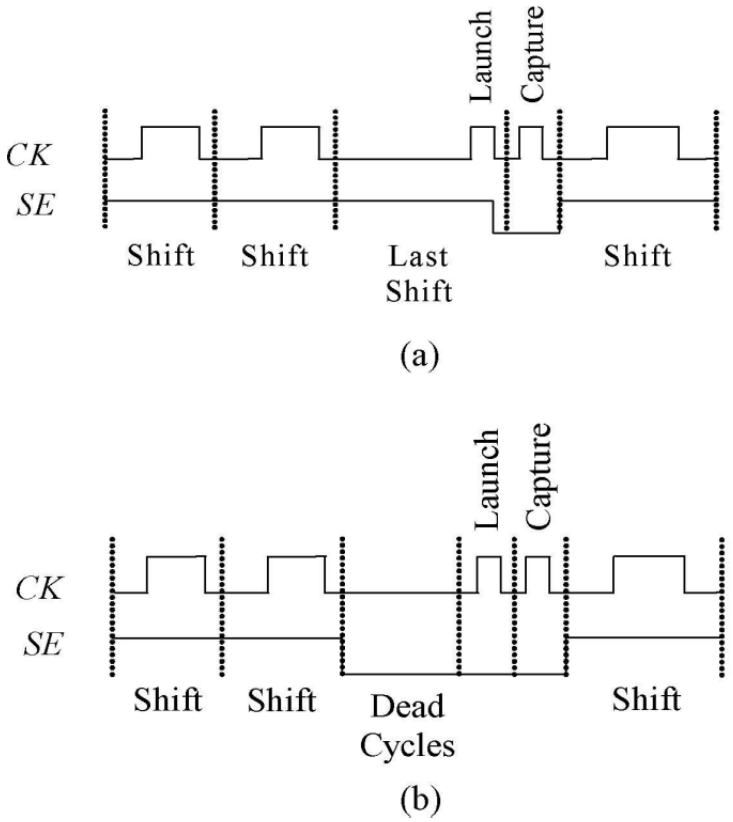
interconnected into one or more scan chains. A330. In scan-test, this sequential input of known data is referred to as shift mode.

When the ASIC is operated in shift mode, each clock pulse pushes a bit of data into the scan chain. This continues until all flip flops in the scan chain are filled with known data. A537 at 2:26-31, A1182. The shift mode then deactivates. Then, one or more clock pulses are applied to the domain as they would be in normal operation, which is referred to as capture mode. A537 at 2:31-36, A1182-1183. The ASIC then returns to shift mode, and with each additional clock pulse, a bit of data is pushed or shifted out as each bit of new data is pushed or shifted in. A537, A1183-1184, A139 at 2:31-39. The shifted out data is then compared with expected results to determine and locate any errors. *Id.* at 2:39-44.

Two options exist for switching between shift and capture modes. The most common uses a scan enable signal. A330-331, A1183-1184. When scan enable is active, the clock domain being controlled is in shift mode, and the incoming clock is sequentially moving data in and out with each clock pulse. When the scan enable signal is inactive during testing, the domain is in capture mode and the incoming clock is sequencing the normal function of the domain with each clock pulse. *Id.* In this way, the scan enable signal acts like a train switch, directing a clock to shift mode or capture mode. This allows the same clock to sequence both shift and capture functions. Alternatively, different clocks following the same path

to a domain can be directed to perform the different functions. *Id.* The second option makes use of a level-sensitive scan latch and is referred to as level-sensitive scan design ("LSSD"). A151 at 26:4-7, A1165 at 143:20-144:1, A365 at 1:9-32. Continuing with the train analogy, LSSD provides a separate path for the clock performing the shift operation. When the shift operation is needed, the latch allows the shift clock through to the domain while stopping the path of the capture clock and vice versa. *Id.*

A single clock pulse applied to the domain under test in capture mode is necessary to test for a stuck-at fault in a clock domain. A141 at 6:17-19, A1190. Since a delay fault test evaluates a flip flop's ability to perform a state transition within a predetermined time, two or more clock pulses are required to complete a delay fault test. *Id.* A first clock pulse is said to launch the transition with the second capturing the result. The clock pulse that launches the transition can be a shift clock pulse – referred to as launch on shift technique – or a capture clock pulse – referred to as launch on capture technique. A723. Diagrams shown below depict these two methods of delay fault testing using a scan enable signal to switch between shift and capture.



A723, A1191.

Historically, the tasks of creating the known data, generating the clock or clocks to perform the shift and capture functions, retrieving the data, and comparing the retrieved data to what was expected were all handled by external automatic test equipment ("ATE"). A1184. More recently, all facets of the scan technique have been built into ASICs, which is referred to as Logic Built-In Self-Test – LBIST, or simply BIST. A722, A1133 at 13:20-16:13, A1186-87. While BIST utilizes the scan technique, scan-test today commonly refers to testing utilizing an ATE, while self-test refers to utilizing the scan technique without an ATE. A141 at 5:52-54.

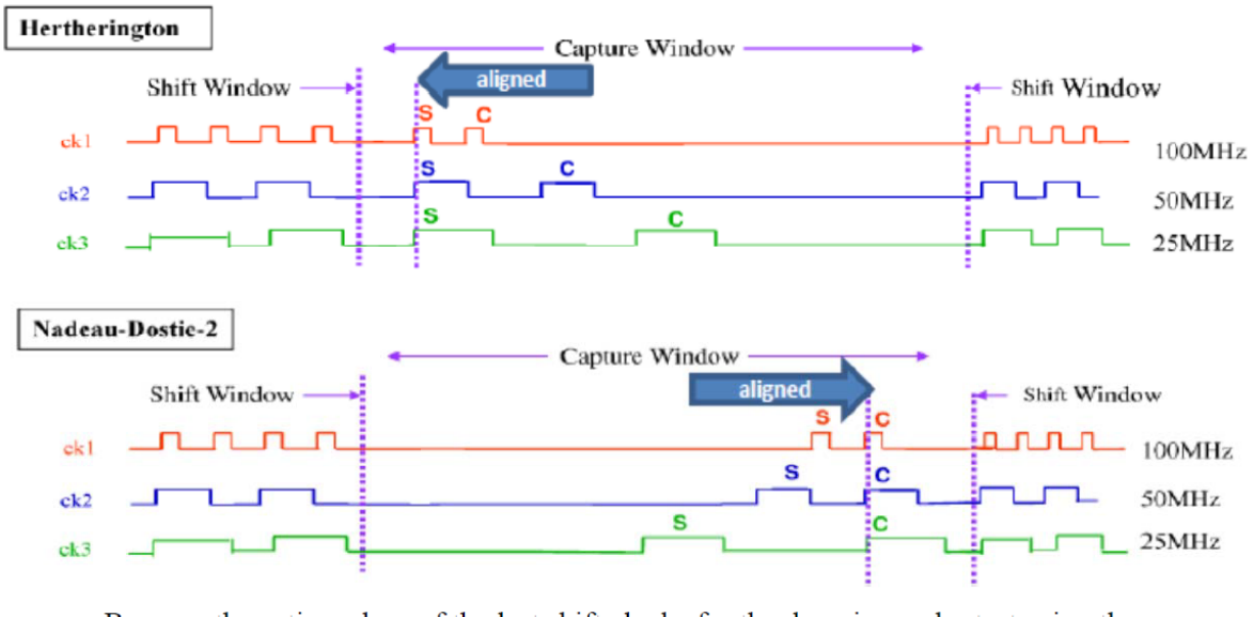
In the place of the ATE externally generating and controlling the test clocks, LBIST is designed to utilize existing resources within the system to generate and control these clocks. A722, A1133 at 13:20-16:13, A1186-87. The ability to utilize each domain's system clock operating at its normal frequency allows delay testing to occur at the speed of the domain's normal operation, something that has become more difficult with an ATE as clock speeds have increased. *Id.* At the time of the invention, an ATE operating at a slower clock speed could handle shifting and other testing operations while the domain's system clock could be used to launch and capture the transition for the delay test. A141 at 5:28-33.

C. The Testing of Circuits with Multiple Clock Domains

Modern ASICs have multiple clock domains operating at synchronous or asynchronous clock speeds.[1] A139 at 1:34-37. While testing domain by domain is possible, the ability to test multiple domains in a single capture window – *i.e.* between shift mode functions – is preferable. A723.

When clocks controlling different domains during testing can easily be aligned – which in turn allows some or all of the clock pulses to be aligned – the prior art taught a number of methods for testing multiple domains in a single capture window.

[1] "Two clock domains are said to be *synchronous* if the active edges of both clocks controlling the two clock domains can be aligned precisely or triggered simultaneously." A722.



A388-389. Clock signals can be aligned when (1) the test uses the same clock to control multiple domains; or (2) the test uses the same clock source to provide clocks to multiple domains and, although the clock speeds are different, they are in a ratio of one another (*e.g.*, 2:1 and 4:1 as shown). A139 at 2:12-30, 54-66, A727. As discussed above in Section I.B., the clock utilized for testing need not be the system clock utilized by the domain during normal operation. The prior art shows that if adequate test clock alignment can be achieved, delay faults can also be tested across interacting clock domains, known as inter-clock domain fault testing. A723, A727-728. In practice, however, it can be difficult to achieve the necessary alignment even with synchronous clocks. A553.

Unintended clock skews[2] occur if expected necessary clock alignment is not secured. A139 at 1:31-47, A236, A568 at 7:65-8:6. Such skews lead to errors in delay fault testing. If a specific delay test awaits a clock pulse to capture a transition, an error can occur when a clock pulse in another interactive domain expected to be aligned occurs too soon. This too-quick clock pulse can erroneously capture the transition. *Id.* To address this problem, prior art suggests when a capture is expected in a domain, all simultaneous clock pulses in any interactive domains that can cause unintended clock skews should be avoided. Clock suppression – a well-known DFT technique – can be used to suppress such simultaneous clock pulses in different domains. A334. The prior art recognized that "[t]his suppression technique is especially useful when clock domains have the same operating frequency and the clocks are synchronous." A541 at 9:8-11, A729.

An alternative to alignment techniques for delay fault testing is to sequentially order the operation of each clock domain under test during capture cycles. By intentionally skewing the capture operation of each domain, no clock domain is operating at the same time, which easily avoids the errors associated with unintended clock skews. A727-728. This staggered approach is the subject

[2] Unintended clock skews should be distinguished from the intended clock skews of the ordered sequence of captured clocks claimed in the patents-in-suit. A139 at 1:51-58.

of the patents-in-suit. The distinction between the two approaches is shown in the diagram below.

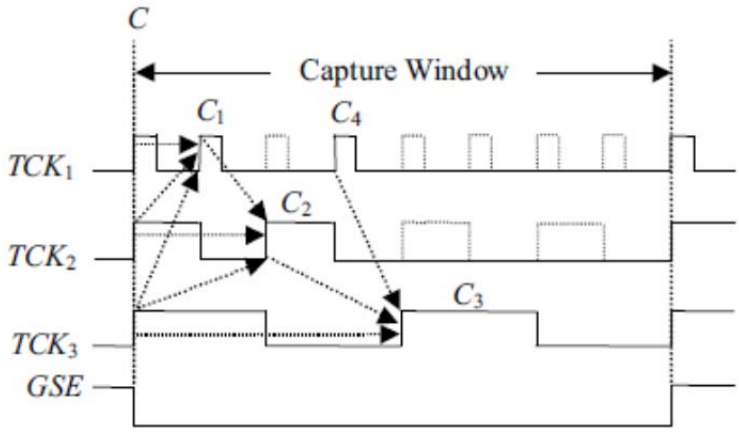


Fig. 9. Launch aligned double-capture.

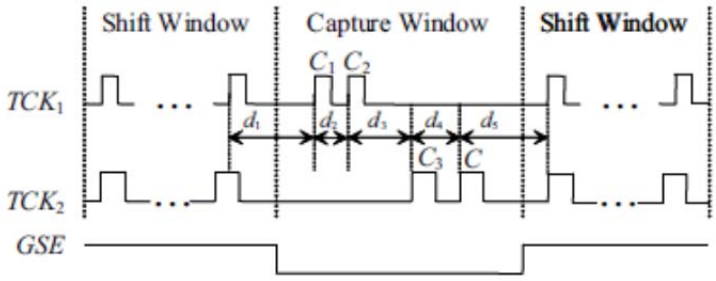


Fig. 10. Staggered double-capture.

A728.

II. THE PATENTS-IN-SUIT

The three patents-in-suit share the same specification.[3] The '213 patent is the parent, the '126 patent is an indirect division of what matured into the '213

[3] Since the three patents-in-suit share the same specification, record cites to the specification will be to the reference's location in the '213 patent unless the reference is directed to one of the other patents only.

patent (A153), and the ‘323 patent is a continuation of the ‘126 patent (A193). Both the ‘213 and ‘323 patents have a single independent apparatus claim and the ‘213 patent also has an independent method claim. A150 at 23:10-46, A151 at 26:15-54, A230 at 22:39-58. Each of these claims is directed to “providing ordered capture clocks to detect or locate faults with N clock domains and faults crossing two clock domains in an integrated circuit . . . .” A150 at 23:11-13, A151 at 26:15-17, A230 at 22:39-42. The ‘126 patent has a single independent claim for a “computer-aided design (CAD) method” directed to the same claimed invention, which also requires “providing ordered sequence of capture clocks.” A190 at 22:38-42. The ‘126 patent allows for the use of the invention in the design of ASICs.

Each of the patents-in-suit is assigned to SynTest. A384. SynTest creates and licenses software tools that practice certain claims of the patents-in-suit. *Id.* Laung-Terng Wang is the lead inventor on each of the patents-in-suit, and founder of SynTest. A390.

A. The Invention

Rather than relying on clock alignment, the patents-in-suit describe the “present invention [as] center[ing] on . . . applying an ordered sequence of capture clocks for capturing output responses in both self-test and scan-test.” A141 at 6:33-37. The specification defines an ordered sequence of capture clocks as

multiple skewed capture clocks. A139 at 1:55-2:58. The specification identifies this feature as distinguishing the present invention from the prior art because "[n]o prior art us[ed] multiple skewed capture clocks . . . to test [for] delay or stuck-at faults [with] two or more capture clock pulses . . . ."[4] A140 at 3:1-4.

The specification contains numerous figures depicting this ordered sequence of capture clocks – intended clock skews – including Figure 3 (showing an ordered sequence of single capture clock pulses for stuck-at fault testing), Figures 10 and 14 (showing an ordered sequence of double capture clock pulses for delay fault testing) depicted below. A116, A123, A127.

[4] The patents-in-suit define an ordered sequence of capture clocks as multiple skewed capture clocks. A139 at 1:54-58 ("none of them can provide multiple skewed capture clocks (or an ordered sequence of capture clocks) in each capture cycle during self-test or scan-test.").

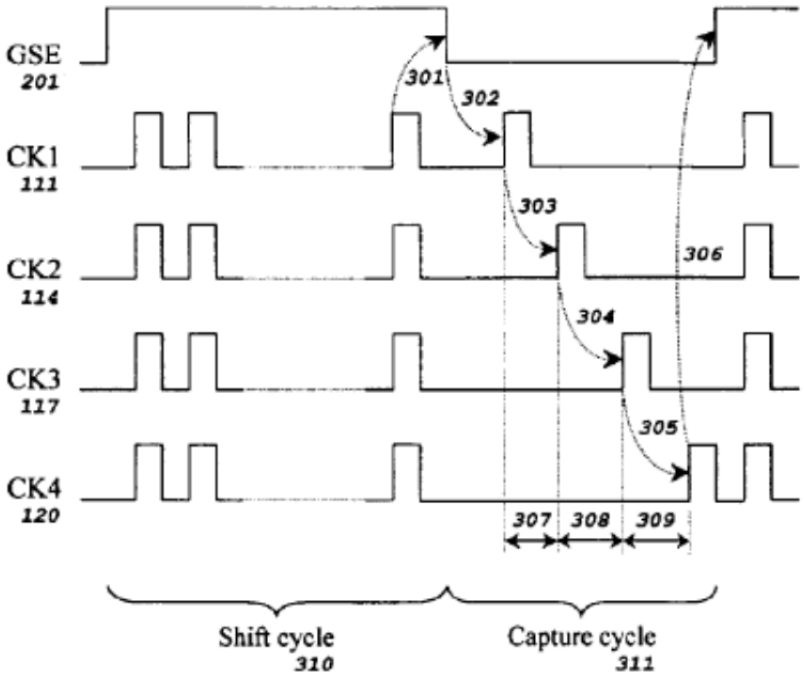


FIG 3 (stuck-at fault test)

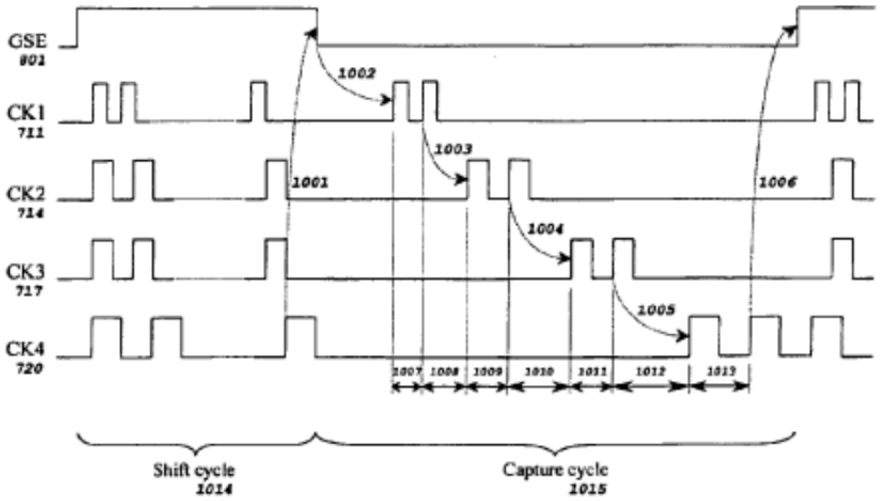


FIG. 10 (delay fault test)

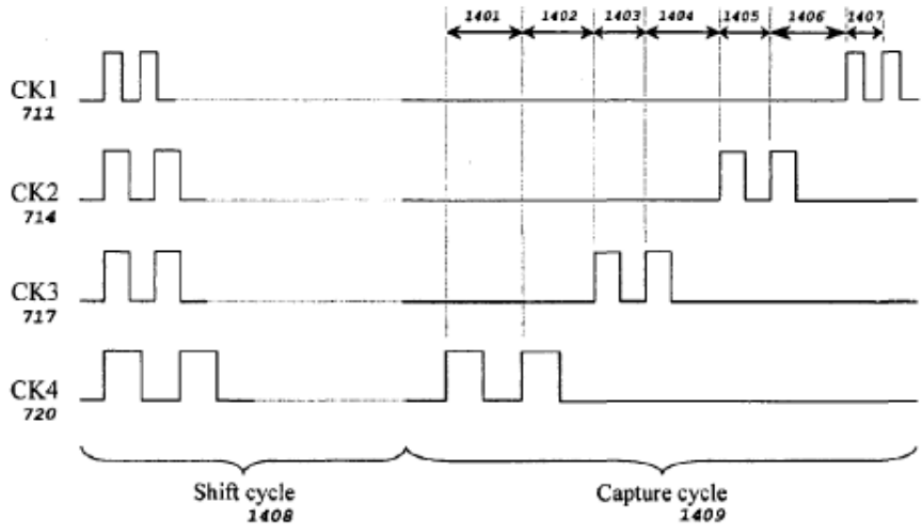


FIG. 14

The specification includes figures showing simultaneous activity in capture cycles of multiple clock domains, such as Figure 11. A124.

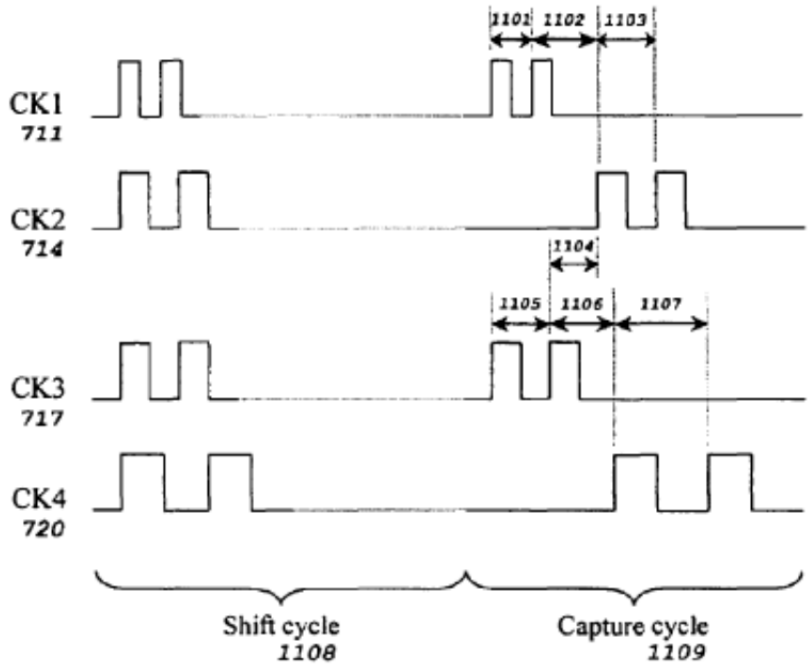


FIG. 11

The specification, however, clearly limits such simultaneous activity to clock domains that do not interact. A141 at 5:44-46. Specifically, "when two clock domains do not interact with each other, they can be tested simultaneously to shorten the capture cycle time."[5] *Id.* Additionally, both the '213 patent and the '323 patent include dependent claims allowing for simultaneous activity if clock domains do not interact. A150 at 24:30-36, A231 at 23:26-32.

B. Background of the Invention

The specification recognizes "a need for an improved method, apparatus, or computer-aided design (CAD) system that allows at-speed or slow-speed testing of faults within clock domains and between any two clock domains using a simple multiple-capture DFT technique." A140 at 3:19-23.

The specification indicates the invention reaches both self-test or scan-test: "[i]n the present invention, both self-test and scan-test techniques are employed to detect or locate stuck-at and delay faults."[6] A141 at 6:8-10. Distinguishing between the two modes, the specification reflects "[w]hen self-test is employed, the multiple-capture DFT system is usually placed inside the integrated circuit [–

[5] Figure 7, to which Figure 11 relates, clearly shows that clocks 1 and 3, with references 711 and 717, do not interact, and, similarly clocks 2 and 4, with references 714 and 720, do not interact. A120.

[6] "The method and apparatus of the present invention will control the multiple-capture operations of the capture clocks in self-test or scan-test mode." A140 at 3:23-26.

LBIST design –] and, thus, all capture clocks are generated internally. When scan-test is employed, the multiple-capture DFT system is usually resided in an ATE and, thus, all capture clocks are controlled externally." A141 at 5:48-54.

The specification explains the advantages and disadvantages of an ordered sequence of capture clocks over the prior art. Among the advantages, the invention does not "need precise timing alignment" of clock pulses to test for intra-clock domain delay faults in order to avoid errors resulting from unintended clock skews. A140 at 3:19-30. Unlike the prior art, however, which, when alignment is achieved, can easily detect delay faults across clock domains, "proper[] ordering of capture clocks and . . . adjustment of relative inter-clock delays" is required for the ordered sequence method to accurately detect delay faults across clock domains. A143 at 9:49-59.

The specification notes that the "DFT approaches . . .proposed [can] take over control of all system clocks" and use them as part of the testing process. A139 at 1:48-50. If a system clock is used, it "can operate at its rated clock speed (at-speed) or [be reconfigured to operate] at a reduced speed (slow-speed)." A143 at 9:37-39. Reconfiguring a clock means the source of the clock is the same, but the clock signal is manipulated to change its frequency or is otherwise manipulated so as to change the clock that performs the function in this testing operation. A143 at 9:17-20.

This distinction is evident in the specification's discussion of Figures 1 and 7. "Since [Figure 1 depicts] a DFT (self-test or scan-test) technique . . . to detect or locate stuck-at faults in the design . . . all system clocks are reconfigured to operate at 10MHz. The reconfigured system clocks are called capture clocks." A143 at 9:17-20. Figure 7, by contrast, depicts an at-speed delay test. "The only difference from FIG 1 is that these clock frequencies will be used directly without alteration in order to implement at-speed self-test or scan test . . . ." A145 at 13:14-16. For at-speed delay testing, a domain's system clock is used without reconfiguration of its frequency. Even when a domain's system clock is operating at-speed, however, it still must be reconfigured to control the number and timing of any clock pulses to order the sequence of the operation at each clock domain.[7] A139 at 1:38-49.

Ordering the sequence of the system clock's operation of the capture cycle allows for true at-speed testing of delay faults at each domain whether applying scan-test or self-test. A59, A723, A728. In scan-test, system clocks can provide the clock signal for the capture operation and an ATE can perform all aspects of

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[7] This need to be able to control the operation of a domain's system clock during testing is elaborated upon in the provisional application underlying the '213 patent.

> One key invention here is that the hardware apparatus must comprise means to halt "capture clocks" until the new stimuli have been fully loaded into all scan registers within the particular clock domain which takes the longest time to complete.

A230.

the scan technique, including generating the shift clock. A141 at 5:30-32. Use of the system clock to perform the capture operation, however, is not required. A141 at 5:57-60, A143 at 9:37-39.

While the specification highlights the distinct advantage of utilizing a domain's system clock for the capture operation, "[t]he shifting frequency, [by contrast,] is irrelevant to at-speed testing." A140 at 4:19-20. Therefore, "[t]he multiple-capture DFT system of the present invention further comprises any method or apparatus for performing the shift operation at any selected clock speed within each clock domain." A140 at 4:31-34.

C. Applying an Ordered Sequence of Capture Clocks

The examples in the specification use a daisy-chain clock-triggering method "to generate and order the sequence of capture clocks one after the other . . . ." A144 at 11:20-22, 11:36-38, A145 at 14:43-45, 14:60-62. The specification discloses one alternative way for automatically triggering a subsequent clock domain – the token-ring clock-enabling technique. A140 at 4:57-60. The specification states that "[i]n the present invention, the multiple-capture DFT system uses a daisy-chain clock-triggering or token-ring clock-enabling technique to generate and order capture clocks." *Id.* For the particular embodiment described, the specification provides that "[s]ince a daisy-chain or token-ring approach is used, the multiple-capture DFT system allows testing of any frequency

domain at a reduced clock speed when this particular frequency domain cannot operate at-speed." A141 at 5:22-25.

Both methods are referred to as automatic clock triggering techniques. In both methods the switching of the scan enable signal from shift to capture triggers the capture operation of the first clock domain, the last capture clock pulse from that first domain then triggers the operation of the next domain, and continuing until the last capture clock pulse of the last domain triggers the scan enable signal to activate the shift operation. A141 at 5:2-17. Obviously, since ASICs with LSSD design do not utilize scan enable signals, neither a daisy-chain clock-triggering nor token-ring clock-enabling approach would work to order the sequence of capture clocks. The patents-in-suit include dependent claims allowing for LSSD. A151 at 26:4-7, A231 at 24:47-50.

The specification identifies a programmable capture window as a third technique for ordering a sequence of capture clocks that can be utilized if increased fault coverage is desired. A141 at 5:37-43. The specification notes that the prior art has used a programmable capture window to order capture clock pulses – as opposed to the operation of each clock controlling separate domains – in the capture window. A140 at 3:5-27.

A programmable technique for ordering the operation of each clock domain differs from the automatic clock triggering techniques in how it orders the

sequence of each clock domain under test. A625-626. In the former, each domain is programmed – utilizing a programmable capture window – to operate at a time no other domain is operating. The latter ensures no overlapping operations by having the completion of a capture sequence in one domain trigger the operation of the next domain.

The claims make no mention of either the daisy-chain clock-triggering method or the token-ring clock-enabling method. The '213 and '323 patents, however, include dependent claims providing that "each said capture clock is programmable . . . to contain said . . . selected number of capture clock pulses for performing said . . . capture operation on all said scan cells within a selected clock domain controlled by said capture clock." A150 at 23:47-52, A230 at 22:62-67.

III. THE FILE HISTORY

The '213 patent has the only relevant file history. On July 21, 2004, two years after the patentees filed their application, the Examiner mails an Office Action rejecting all claims as obvious in light of two patents to Nadeau-Dostie, *et al*. (Patent Nos. 6,442,722 and 5,349,587 (collectively, "Nadeau-Dostie")). A254, A280.

The Examiner receives the patentees' response on October 25, 2004. Responding to the obviousness objection, the patentees first restate their invention:

> For at-speed testing, the application proposed using a delay test technique by applying two or more capture

> clocks, each controlling one clock domain and comprising two or more capture clock pulses (without any shift clock pulse), in a sequential order (ordered sequence), during a capture operation. This delay test technique is, in general, called "broadside" or "double-capture"….

A279 (emphasis in original). The patentees then note the Nadeau-Dostie prior art taught a launch on shift approach, which was something completely different. A280. To draw out this distinction, the patentees amend the claim language to reflect "each said selected capture clock must contain at least one said capture clock pulse and does not contain any said shift clock pulses during the capture operation." A255.

On January 27, 2005, the Examiner mails a further Office Action. A283-284. Among other things, the Examiner rejects all pending claims as not enabled and indefinite. Specifically, the Examiner cites the added language "each said selected capture clock must contain at least one said capture clock pulse **and does not contain any said shift clock pulse**." A288 (emphasis on original).

> The Examiner asserts that any clock is comprised of only pulses belonging to the particular clock and cannot be comprised of pulses belonging to any other clock. Hence a capture clock is comprised of only pulses belonging to the capture clock, *i.e.*, capture clock pulses, and cannot be comprised of shift clock pulses because shift clock pulses belong to a shift clock not a capture clock. The Examiner…points out that the Examiner does not believe that is what the Applicant intends anyway.

Id.

The Examiner reasserts his obviousness objection to the amended claims, citing Nadeau-Dostie again. A289.

In response, the patentees request an interview, and on March 31, 2005, the Examiner meets with Dr. Wang and his counsel. A322, A948. In his summary of the interview, the Examiner writes "[t]he [patentees] clearly explained the invention and how the [patentees'] invention overcame the current Prior Art. The [patentees] agreed to submit a proposed amendment to [what became claim 1]." A948.

On April 5, 2005, the Examiner receives the patentees' amendment in response to the January 27, 2005 Office Action and interview. A572. Responding to the enablement and indefiniteness challenges, the patentees state they

> [a]ppreciate[] the Examiner's comments regarding the language: "and does not contain any said shift clock pulse during a capture operation," and ha[ve] deleted same from the claims, thereby obviating the 35 U.S.C. §112, first and second paragraph rejections.
>
> As a further result, [the patentees]…define[] shift clock pulse "in scan mode" and capture clock pulse "in normal mode". This is to clarify the Examiner's concern that a capture clock should contain only capture clock pulses, and a shift clock should contain only shift clock pulses.

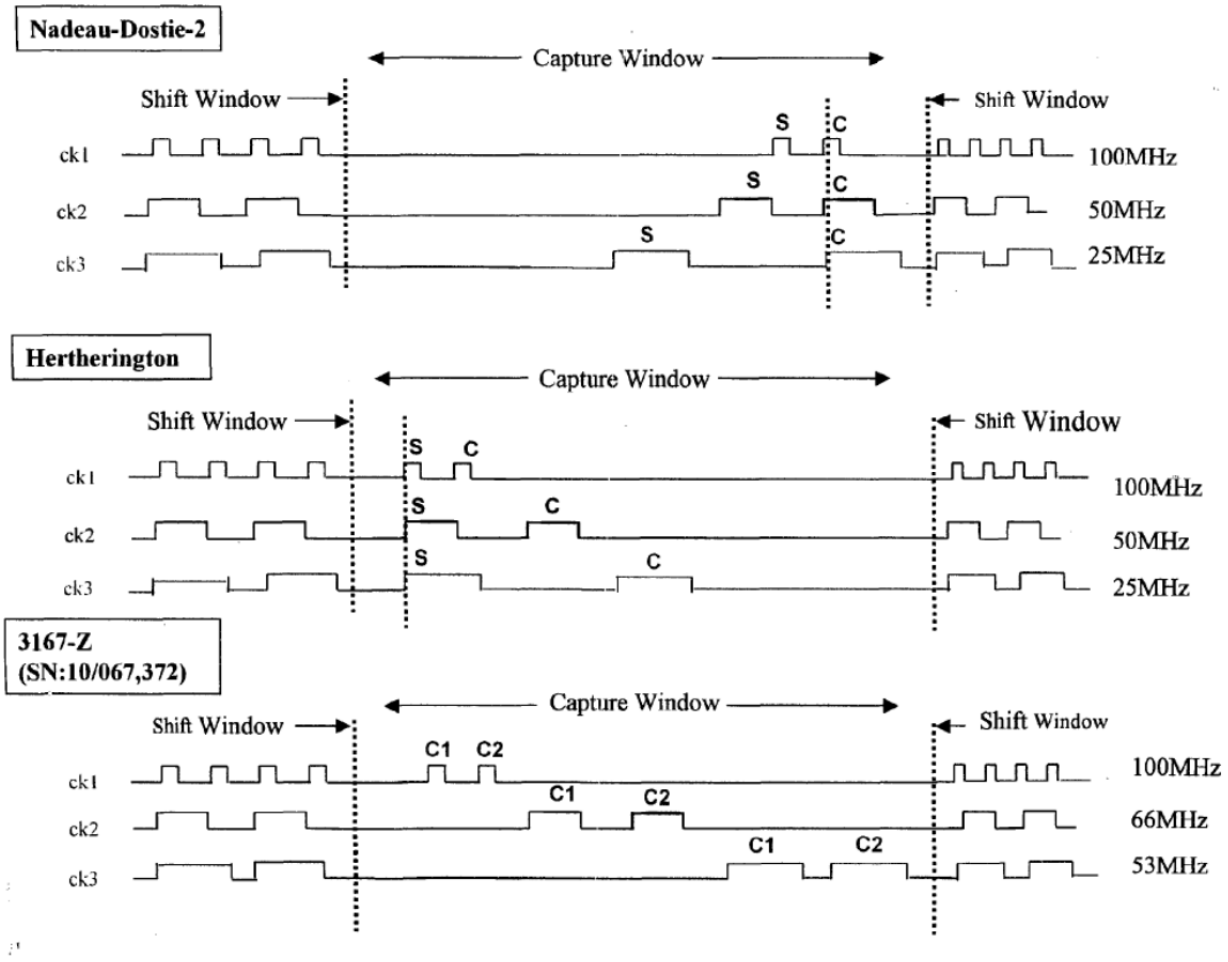
A588-589. The patentees continue

> In many designs, a clock domain may be only controlled by one test clock. Thus, this test clock will contain clock pulses applied in scan mode (hence shift clock pulses)

> and clock pulses in normal mode (hence capture clock pulses).
>
> Applicant happened to call the test clock "the capture clock", which inadvertently and unfortunately has created some confusion.

A589.

With respect to the obviousness challenge, patentees recount the Examiner's interview with Dr. Wang, where Dr. Wang discussed the unintended clock skew problem associated with the aligned approach disclosed by Nadeau-Dostie. A590-591. "Most importantly, [the patentees recount,] the present invention can allow testing of asynchronous clock domains." A591. The patentees attach the timing waveform Dr. Wang provided the Examiner to explain the difference between their invention, which did not require any alignment, and the prior art, including both Nadeau-Dostie and the Hertherington Article, which require alignment. A590.



A593.

The Examiner issues a notice of allowance without comment following this amendment. A704.

IV. CLAIM CONSTRUCTION ORDER

On November 21, 2012, SynTest filed in the Northern District of California its complaint against Cisco alleging infringement of the patents-in-suit. A38. Upon consent, United States Magistrate Judge Paul S. Grewal presides. A41-43.

Following briefing, the District Court held a tutorial and claim construction hearing on the afternoon of October 18, 2013. A1130. At the end of the hearing, the District Court departed from his normal practice of immediately issuing constructions, indicating that an order would issue shortly. A1169 at 159:20-161-15. The District Court also indicated that he would "very likely…follow that order up with [his] reasoning and a more consider[ed] opinion that will be useful... for any further appeal or any other issues you may want to take upstairs…." A1170 at 161:12-15.

While the District Court issued his claim construction order on October 22, 2013 (A1171), he did not provide his reasoning in support of the order until June 9, 2014 (A36). Only a subset of the terms construed by the District Court are relevant to this appeal.

A. Dispute #2: Providing Ordered Capture Clocks

The District Court construes the term "providing ordered capture clocks" (The '213 patent (claims 1 and 29), the '126 patent (claim 1) and the '323 patent (claim 1)) as "**triggering** a capture clock pulse in at least one clock domain **in response to a capture clock pulse in another clock domain**." A18 (emphasis added).

1. Triggering

Citing the specification's use of the phrase "in the present invention" in connection with its discussion of both the "daisy-chain clock-triggering" and "token-ring clock-enabling" techniques, the District Court concludes "the asserted patents specifically describe the 'invention' as using either [of these] techniques." A18. Since, according to the District Court, "both techniques require generation of capture clock pulses for one clock domain in direct response to a capture clock pulse in another clock domain," it is appropriate to further limit the construction of triggering to a triggering in "direct response to a capture clock pulse in another clock domain," *i.e.*, an automatic clock triggering technique. A19.

As further support, the District Court identifies that claims in both the '126 and '323 patents use the term triggered, albeit in a different context. Specifically, both patents claim "selected capture clocks placed in a sequential order such that all clock domains are never triggered simultaneously during a capture operation." A1128 at 22:50-36, A1090 at 23:19-24:2. The District Court also cites for support the patentees' generic use of triggering during prosecution to distinguish prior art from what matured into the '213 patent. A20.

In a footnote, the District Court discounts the specification's identification of a programmable capture window as simply being a refinement of the "daisy-chain

clock-triggering" and "token-ring clock-enabling" techniques rather than an independent method. *Id.* at n. 37.

2. Capture Clock

In rejecting SynTest's contention that "capture clock" be construed as a "test clock," the District Court first notes SynTest's prior agreement that a capture clock was a reconfigured system clock. A21. Not relying on this prior agreement, the District Court concludes the record supports construing a capture clock to be a reconfigured system clock. *Id.*

The District Court dispenses with SynTest's citation to the prosecution history where the patentees inform the Examiner that they have defined capture clock to mean test clock, and understands how this causes confusion.

> While it is therefore true that the capture clock claimed in the asserted patents can be used during testing, it does not follow that every "test clock" is a capture clock as claimed in the asserted patents. Indeed, not every test clock is a "reconfigured system clock," which the parties have agreed and the patents confirm is the claimed "capture clock."

A21.

While the District Court accepts that the patents-in-suit embrace both scan-test and self-test, he concludes that this is of no import. A20. "The patents explain that the system clocks can be generated inside of the circuit being tested or can be received from an external source at one of their input pins. Whether generated

internally or controlled externally, the capture clocks are reconfigured system clocks, and they are clocks that contain both shift clock pulses and capture clock pulses, depending on the operational mode." A22. The notion of a capture clock containing both shift clock pulses and capture clock pulses is taken from the preamble of both independent claims of the '213 patent. In his claim construction order, however, the District Court construes that neither of these preambles are limiting. A15-17.

B. Dispute #3.

The District Court construes dispute term #3:

> "applying an ordered sequence of capture clock pulses to all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture clock pulses comprising at least two capture clock pulses from two or more selected capture clocks, for controlling two or more clock domains, in a sequential order" [The '213 patent (claims 1 and 29)]

as

> "applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode by **triggering a capture clock pulse in the latter clock domain in response to a capture clock pulse in the former clock domain**"

A23 (emphasis added). The only issue with respect to this construction relevant to this appeal is the "ordered sequence of capture clock pulses." The District Court simply re-adopts his reasoning for applying an automatic clock triggering limitation.

C. Dispute #4.

The District Court construes dispute term #4:

> "applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least a plurality of capture clock pulses from two or more selected capture clocks placed in a sequential order such that all clock domains are never triggered simultaneously during a capture operation" [The '126 patent (claim 5) and the '323 patent (claim 1)]

as

> "applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode **by triggering a capture clock pulse in the latter clock domain in response to a capture clock pulse in the former clock domain such that all clock domains are never triggered simultaneously during a capture operation**"

A26. Again, the only issue with respect to this construction relevant to this appeal is the "an ordered sequence of capture clocks." The District Court simply re-adopts his reasoning for applying an automatic clock triggering limitation.

D. Dispute #8.

The District Court construes dispute term #8:

> "each shift clock pulse comprising a clock pulse applied in scan mode" [The '213 patent (claims 1, 29) and the '126 patent (claim 1)]

as

> "each **shift clock pulse comprising a pulse of the capture clock** at a frequency that need not be the same as the normal operating frequency of the domain's system clock"

A32 (emphasis added). The District Court's construction clearly limits the source of shift clock pulses to pulses of the capture clock. His reasoning, however, indicates that such a limitation is inappropriate. Rejecting "Cisco's attempt to limit the clock that can generate this pulse to a reconfigured system clock," the District Court states Cisco's "construction ignores the specification, which identifies the reach of the invention to embrace both self-test and scan-test. Additionally, the specification recognizes that separate clocks can be responsible for shift clock pulses and capture clock pulses." A32.

E. Dispute #9.

The District Court construes dispute term #9:

> "each capture clock pulse comprising a clock pulse applied in normal mode" [The '213 patent (claims 1, 29) and the '126 patent (claim 1)]

as

> "each capture clock pulse comprising a pulse **of the capture clock** at a frequency that need not be the same as the clock when generating shift clock pulses"

A33 (emphasis added). Again, the issue is the District Court's addition of the limitation that the clock pulse come from the capture clock. The District Court simply adopts its reasoning in support of its construction of term #8.

F. Dispute #10.

The final term for construction –

> **means for generating and shifting-in** N test stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly **during a shift operation**

– presented a means-plus-function limitation governed by 35 USC § 112(f). The District Court first notes the parties' agreement on the two functions "(1) generating N test stimuli and (2) shifting in N test stimuli to all said scan cells." A34.

With respect to the structure for each function, the District Court rejects Cisco's effort to limit the invention. A34-35. For example "Cisco identifies the 'capture clock' as the structure for the second element citing that 'during each shift cycle' a 'series of pulses' are 'applied through capture clocks' to shift stimuli to all scan cells within all clock[] domains." A35. The District Court finds "inappropriate" Cisco's "effort to read out scan-test" by citing "to the capture clock" as the structure, noting "[t]he specification . . . recognizes that separate

clocks can generate shift clock pulses and capture clock pulses." *Id.* Similarly, the District Court rejects Cisco's effort to limit the structure to one requiring a scan-enable signal. "While the use of a scan-enabled signal may be the most common way to shift data in and out of a scan chain during test, the specification makes clear that the 'multiple-capture DFT system of the present invention further comprises any method or apparatus for performing the shift operation at any selected clock speed within each clock' domain." *Id.*

The District Court construes two separate structures for the function generating N test stimuli: "[i]f self-test – the PRPG with or without a phase shifter. If scan-test – the ATPG." A34. Similarly, the District Court construes two separate structures for the function shifting-in N test stimuli: "[i]f self-test – the DFT system. If scan-test – the ATE." *Id*.

V. JUDGMENT

To avoid a waste of judicial resources, SynTest, on October 22, 2013, agreed to stipulate to a judgment based on the District Court's issued construction. A3, A1394. While the District Court initially entered judgment on this stipulation on November 18, 2013, he vacated that judgment pending his memorandum order supporting his constructions. A1403, A1410, A1412.

On June 9, 2014, the District Court issued a claim construction order that included reasoning for his constructions. A8. Thereafter on June 12, 2014, the

District Court entered judgment based on the parties' prior stipulation. A1. Cisco specifically cites two bases for non-infringement.

First, with respect to the ordered sequence of capture clocks, Cisco states that "its Accused Instrumentalities do not practice th[is] limitation as construed by the Court at least because they trigger a domain's capture clock pulses based on the number of cycles that have occurred in a common reference clock, rather than triggering a capture clock pulse in at least one clock domain in response to a capture clock pulse in another clock domain." A4-5.

Second, with respect to the District Court's construction of "each shift clock pulse comprising a clock pulse applied in scan mode" and "each capture clock pulse comprising a clock pulse in normal mode," to which the District Court added the limitation that such pulses must come from the capture clock, "Cisco assert[ed] that the clock that comprises capture clock pulses in the Cisco Accused Instrumentalities does not also comprise shift clock pulses." A5.

SUMMARY OF ARGUMENT

In three instances, the District Court's constructions impose limitations on the ordinary meaning of terms or phrases in dispute. SynTest asks this Court to independently determine whether the claim language, specification, and file history meet the exacting standard necessary to impose such limitations.

First, in construing an "an ordered sequence of capture clocks" and an "ordered sequence of capture clock pulses" Cisco argued, and the District Court agreed, to limit the techniques for achieving an order sequence to automatic clock triggering, eschewing any programmable techniques. The ordinary meaning of "an ordered sequence," however, would not impose such a limitation. While the specification uses the phrase "in the present invention" in connection with discussions of automatic clock triggering techniques, such a reference alone is insufficient to import a limitation. Here, both the specification and dependent claims reference achieving the requisite ordering with programmable or LSSD techniques. Furthermore, the file history does not reflect any effort by the patentees to limit available techniques to automatic clock triggering.

Second, Cisco argued, and the District Court agreed, to limit the ordinary meaning of "a pulse" to a pulse of the capture clock. The District Court's own reasoning, however, fails to support the construction. As recognized by the District Court, the specification supports that the source for shift clock pulses need not be the same as the source for capture clock pulses. Similarly, and consistent with the comments of the Examiner during prosecution, a capture clock is made up of capture clock pulses and not shift clock pulses.

Third, Cisco argued, and the District Court agreed, to limit the ordinary meaning of "capture clock" to a "reconfigured system clock." While consistent

with the specification, SynTest had agreed that "capture clock" could be construed as a "reconfigured system clock," in both briefing and oral argument SynTest demonstrated why imposing such a limitation was inappropriate. SynTest offered alternative constructions, including that capture clock could be construed as a "clock with capture clock pulses" or as a "test clock." The specification provides that "in the present invention" the source for the capture clock can be either internal – indicating that the clock is a reconfigured system clock – or external from an ATE. In the file history, the patentees acknowledged the confusion caused by their defining "test clock" as "capture clock," which they attempted to rectify by amending certain claim language. Again, nothing in the file history or specification meets the exacting standard required to limit the construction of "capture clock" to simply a "reconfigured system clock."

STANDARD OF REVIEW

This Court recently reaffirmed "that patent claim construction receives *de novo* determination on appeal, that is, review for correctness as a matter of law. Such review is conducted on the administrative record and any additional information in the record of the district court, and is determined without deference to the ruling of the district court." *Lighting Ballast Control v. Philips Electronics North America Corp.*, 744 F.3d 1272, 1292 (Fed. Cir. 2014) ("we are not persuaded that discarding *de novo* review would produce a better or more reliable

or more accurate or more just determination of patent claim scope."). Where parties have stipulated to a judgment following claim construction, and this Court concludes a construction that formed the basis of the stipulated judgment is incorrect, the judgment should be reversed. *Paragon Solutions, LLC v. Timex Corp.*, 566 F.3d 1075, 1093 (Fed. Cir. 2009).

ARGUMENT

I. THE DISTRICT COURT'S CONSTRUCTIONS OF DISPUTES #2, #3 AND #4 INAPPROPRIATELY LIMIT THE WAYS OF ACHIEVING AN ORDERED SEQUENCE OF CAPTURE CLOCKS

The specification broadly characterizes an "ordered sequence of capture clocks" as "multiple skewed capture clocks" without regard for the method used to achieve the intended skew. A139 at 1:54-58. The specification identifies this feature as distinguishing the claimed invention from the prior art. A140 at 3:1-4.

At the time of the invention, alternatives to the daisy-chain clock-triggering and token-ring clock-enabling techniques for ordering capture clock pulses were known in the art. One alternative is a programmable capture window, the technique Cisco implements with the accused instrumentalities. A4. This technique is discussed in the specification,[8] in dependent claims,[9] and in the intrinsic record.[10]

[8] A140 at 3:8-11, A141 5:39-41.

Disputes #2, #3 and #4 address an "ordered sequence of capture clocks" or an "ordered sequence of capture clock pulses." Ordinary meanings of the disputed phrases include (1) "providing two or more test clocks in a given order" (A18) or simply (2) "providing multiple skewed capture clocks" (A139 at 1:55-57). There can be no dispute that the ordinary meaning of an ordered sequence of capture clocks would encompass the use of a programmable capture window. A727, 729.

The District Court's construction limits the ways of ordering to "triggering a capture clock pulse in at least one clock domain in response to a capture clock pulse in another clock domain"[11] and "triggering a capture clock pulse in the latter clock domain in response to the capture clock pulse in the former clock domain."[12] Absent an exception, the District Court limiting construction must fail. *Hill-Rom Services, Inc. v. Stryker Corp.* – F.3d – , 2014 WL 2898495, *1 (Fed. Cir. 2014) ("Claim terms are generally given their plain and ordinary meanings to one of skill in the art when read in the context of the specification and prosecution history."). For "[i]t is improper for a court to add extraneous limitations to a claim, that is limitations added wholly apart from any need to interpret what the patentee meant

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[9] A150 at 23:47-56, A230 at 22:62-67.

[10] A335, A549-550.

[11] Dispute #2 relating to claim language in claims 1 and 29 of the '213 patent. A11.

[12] Dispute #3 relating to claims 1 and 29 of the '213 patent and Dispute #4 relating to claim 5 of the '126 patent and claim 1 of the '323 patent. A23, A26.

by a particular word or phrase in the claim." *Hoganas AB v. Dresser Indus. Inc.*, 9 F.3d 948, 950 (Fed. Cir. 1985); *Flo Healthcare Solutions, LLC v. Kappos*, 697 F.3d 1367, 1375 (Fed. Cir. 2012) ("it is not proper to import from the patent's written description limitations that are not found in the claims themselves").

Because this Court will "indulge a 'heavy presumption' that a claim term carries its ordinary and customary meaning," it is incumbent upon Cisco, who seeks the deviation, to prove the patentees' "clear intent to depart from the ordinary meaning" by application of an exception. *Starhome GmbH v. AT & T Mobility LLC*, 743 F.3d 849, 857 (Fed. Cir. 2014). "There are only two exceptions . . . : 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of the claim term either in the specification or during prosecution." *Thorner v. Sony Computer Entertainment Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). "The standard" to satisfy is "exacting." *Id.* at 1366. "To act as its own lexicographer, a patentee must "clearly set forth a definition of the disputed claim term" other than its plain and ordinary meaning." *Id.* at 1365 (quoting *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed.Cir.2002)). "To constitute disclaimer, there must be a clear and unmistakable disclaimer." *Id.* at 1366-1367.

Cisco prevailed on the District Court making three arguments. **First**, Cisco contends the patentees conveyed a "clear intention" to limit the invention to these

two techniques by the specification's use of the phrase "in the present invention" in proximity of discussions of the daisy-chain clock-triggering and token-ring clock-enabling techniques. **Second**, and to bolster this alleged clear intent, Cisco argues that during prosecution the patentees relied on the use of these automatic clock triggering techniques to distinguish their invention from the prior art. **Third**, Cisco argues the specification belittles the programmable technique. Cisco's proffer is wholly insufficient under this Court's controlling case law, especially when considered with the contrary evidence.

As a preliminary matter, the term "triggering" in and of itself is not the flaw in the construction Cisco asks this Court to affirm. It is the further limitation that such triggering be automatic – attributable to the actions of the capture clock pulse of another domain. As the District Court's own order recognizes, triggering can have a generic meaning that would not limit the claims to an ordering utilizing either the daisy-chain clock-triggering and token-ring clock-enabling techniques. A20. For example, the action of the programmable capture window used by Cisco triggers the operation of each clock domain.

A. Despite the Use of the Phrase "Present Invention," Ordering Should Not be Limited to the Daisy-Chain Clock-Triggering or the Token-Ring Clock-Enabling Techniques

Although reluctant to read a preferred embodiment as a limitation, this Court's reluctance is somewhat tempered when "the inventors use of the term 'the present invention' rather than 'a preferred embodiment.'" *Trading Technologies Intern., Inc. v. eSpeed, Inc.*, 595 F.3d 1340, 1353 (Fed. Cir. 2010) ("This court takes some comfort against this risk from the inventors' use of the term 'the present invention' rather than 'a preferred embodiment . . . ."). Even "clear language characterizing [an embodiment as] 'the present invention'[, however,]. . . must be read in context of the entire specification and the prosecution history." *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094-95 (Fed. Cir. 2003) ("Although the above references, taken alone, may suggest some limitation of 'bus' to a multiplexing bus, the remainder of the specification and prosecution history shows that Rambus did not clearly disclaim or disavow such claim scope in this case.") (citations omitted).

"It is true that, in some circumstances, a patentee's consistent reference to a certain limitation or a preferred embodiment as 'this invention' or the 'present invention' can serve to limit the scope of the entire invention, particularly where no other intrinsic evidence suggests otherwise." *Absolute Software, Inc. v. Stealth*

Signal, Inc., 659 F.3d 1121, 1136 (Fed. Cir. 2011); *SciMed Life Systems v. Advanced Cardiovascular*, 242 F.3d 1337 1344 (Fed Cir. 2001) ("The words 'all embodiments of the present invention' are broad and unequivocal."). Similarly, where the specification describes all features of the invention as a whole following the use of the phrase "present invention," this Court has found such a description to limit the scope of the invention. *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007) ("When a patent thus describes the features of the 'present invention' as a whole, this description limits the scope of the invention")*; accord Regents of Univ. of Minnesota v. AGA Medical Corp.*, 717 F.3d 929, 938 (Fed. Cir. 2013).

"On the other hand, [this Court has] found that use of the phrase 'present invention' or 'this invention' is not always so limiting, such as where the references to a certain limitation as being the 'invention' are not uniform, or where other portions of the intrinsic evidence do not support applying the limitation to the entire patent." *Absolute Software, Inc.*, 659 F.3d at 1136 (patent does not uniformly refer to one-call-per-time period as being coextensive with the entire invention); *see also Voda v. Cordis Corp*., 536 F.3d 1311, 1320-22 (Fed. Cir. 2008) (although parts of the specification referred to a certain embodiment as the "present invention," the specification did not uniformly refer to the invention as being so limited, and the prosecution history did not reveal such a limitation).

Stated simply, "'[a]bsent a clear disclaimer of particular subject matter, the fact that the inventor may have anticipated that the invention would be used in a particular way [– as would be inferred from the use of "present invention" –] does not mean that the scope of the invention is limited to that context.'" *Liebel-Flarsheim Company v. Medrad, Inc.*, 358 F.3d 898, 909 (Fed. Cir. 2004) (quoting *Northrop Grumman, Corp. v. Intel Corp*., 325 F.3d 1346, 1355 (2003) (alterations added)).

The common specification for the patents-in-suit uses the phase "present invention" 50 times, albeit to refer to a number of different features and embodiments. *Compare Netcraft Corp. v. eBay, Inc.*, 549 F.3d 1394, 1398 (Fed. Cir. 2008) ("use of the phrase 'the present invention' does not 'automatically' limit the meaning of claim terms in all circumstances . . . however, . . . the common specification's repeated use of the phrase 'the present invention' describes the invention as a whole" and limits the construction). This lack of consistent use of "present invention" distinguishes this case from *Netcraft* and its progeny. *Compare Marine Polymer Technologies, Inc. v. HemCon, Inc*., 672 F.3d 1350, 1359 (Fed. Cir. 2012) (consistent use). Similarly, in no instance are all features of the invention, including the automatic clock triggering techniques, collected under any single use of that phrase. *Compare Verizon Services Corp.*, 503 F.3d at 1308 ("When a patent thus describes the features of the 'present invention' as a whole,

this description limits the scope of the invention."). Nothing supports that the mere repeated use of the term "present invention," as opposed to the repeated identification of an embodiment or feature as the "present invention," demonstrates a patentee's clear intent to limit an invention. Rather, differing references to features indicate the patentee's preferred use, not sufficient to read a limitation on ordinary meaning. *Liebel-Flarsheim*, 358 F. 3d at 909 (using of preferred invention indicated anticipated use and not a limitation).

Only two of 50 references to "present invention" relate to a method for ordering capture clocks:

> In the present invention, the multiple-capture DFT system uses a daisy-chain clock-triggering or token-ring clock-enabling technique to generate and order capture clocks.

A140 at 4:57-60.

> The multiple-capture DFT system in the present invention further comprises applying an ordered sequence of capture clocks and operating each capture clock at its selected clock speed in the capture operation (cycle). The ordered sequence is applied one-by-one using the daisy-chain clock-triggering or token-ring clock-enabling technique.

A141 at 5:33-39.

The specification highlights the advantage of utilizing these automatic clock triggering functions – "[o]ne major benefit of using this approach is that the test results are repeatable no matter what clock speed will be used for each capture

clock" (A140 at 4:60-62) – as well at their disadvantage – "it could be difficult to precisely control the relative clock delay between two adjacent capture clocks for testing delay faults between clock domains." A140 at 4:63-65. The specification further provides that if increased fault coverage is desired, the order of capture clocks is programmable: "[t]he order of these capture clocks is further programmable, when it's required to increase the circuit's fault coverage." A141 at 5:39-43.[13]

The District Court seizes on "further," and concludes, without support, that "further" refers to using the programmable technique in conjunction with the automatic clock triggering techniques. A20 at n. 37. Nothing in the specification or in the record, however, indicates that the two techniques can be so combined. Rather, the specification makes clear that a deficiency of the automatic clock triggering technique – decreased fault coverage – can be addressed by using the programmable method instead, which allows for increased fault coverage.

While claims in the patents-in-suit make generic use of "triggering" with the claim limitation "all clock domains are never triggered simultaneously during the capture operation," there is no mention in the claims of any automatic clock

[13] While the art recognizes automatic clock triggering techniques are "more suitable for testing asynchronous clock domains," programmable capture clock windows "can also be used to generate timing waveforms for testing asynchronous designs." A729.

triggering technique. A191 at 23:18-24:2, A230 at 22:50-56; *see Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1325 (Fed. Cir. 2003) ("The danger of improperly importing a limitation is even greater when the purported limitation is based upon a term not appearing in the claim."). By contrast, two of the patents-in-suit contain relevant dependent claims specifically recognizing that the capture clocks are programmable. A150 at 23:47-56, A230 at 22:63-23:4. Obviously, where a specific method is identified in a dependent claim, that method must be among the methods – *e.g.* how capture clocks can be ordered – covered by the independent claim. *Wright Medical*, 122 F.3d 1440, 1445 (Fed. Cir. 1997) ("we must not interpret an independent claim in a way that is inconsistent with a claim which depends from it").

The specifications' other uses of "the present invention" provide further support for the patentees' lack of intent to limit their invention to features under that nomenclature. For example, the specification makes repeated reference to the "present invention . . . using only one global scan enable (GSE) signal." A140 at 4:31-35, A141 at 6:33-35 ("the present invention centers on using one global scan enable (GSE) signal"). The patents-in-suit claims, however, reach ASICs with LSSD storage elements, a design that does not make use of any scan enable signal to switch between shift and capture functions. A151 at 26:4-7, A231 at 24:48-51. To read "present invention" as requiring use of a global scan enable signal, as well

as automatic clock triggering, which also requires a global scan enable signal, would read out of the dependent claim allowing for use of an LSSD.[14] *Wright Medical*, 122 F.3d at 1445.

In sum, the patentees' use in the specification of "present invention" in conjunction with automatic clock triggering techniques alone is insufficient to establish the patentees' clear intent to limit the method of ordering to automatic clock triggering, and other portions of the specification simply bolster this lack of intent.

B. The Prosecution History Makes No Mention of Daisy-Chain Clock-Triggering or Token-Ring Clock-Enabling Techniques

Nothing in the prosecution history supports Cisco's effort to narrow the meaning of "an ordered sequence of capture clocks." To the contrary, the prosecution history supports no limitation on the methods for achieving such an ordered sequence.

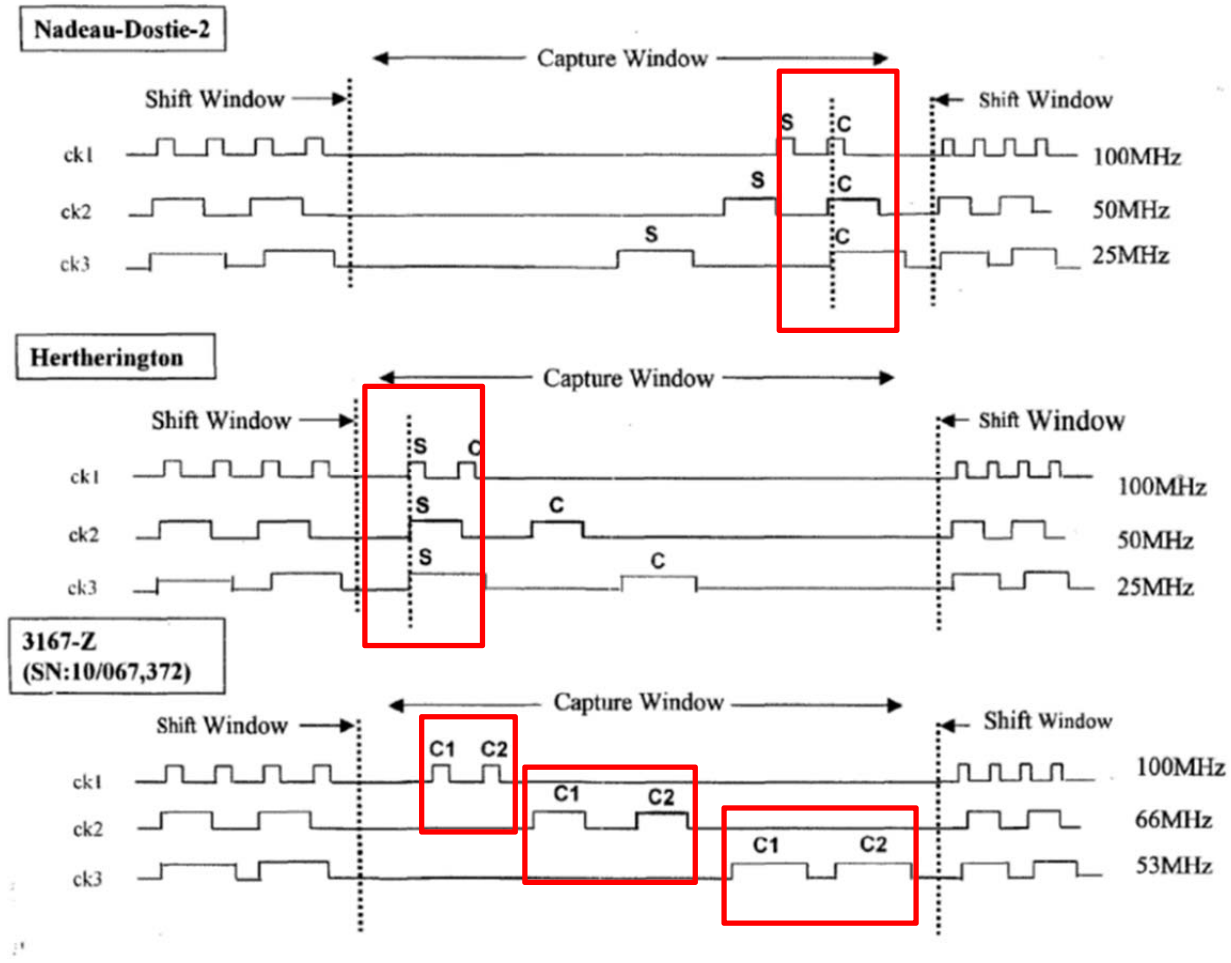
Below, Cisco plied that the "distinction made [during prosecution] by Applicants between the claimed invention and the prior art is that the alleged 'invention' applied the ordered sequence of capture clocks using the daisy-chain or

[14] Curiously, while the District Court's construction limits the methods of ordering to automatic clock triggering techniques, the District Court, in its construction of Dispute #10 explicitly recognized that the invention did not require use of a scan-enable signal, which is required for each of the automatic clock triggering techniques. A35.

token-ring technique." A667 at 5:6-9. Cognizant of Cisco's error, the District Court tempers that "the patentees relied on the claim requirement of 'applying an ordered sequence of capture clock pulses' in 'sequential order' during prosecution to distinguish prior art." A20 at 4-5. This is true. Indeed, logic extends to the District Court's conclusion – "[b]ecause [of this,] using of the triggering term is appropriate in the court's construction." *Id.* The District Court continues "the foundation of the asserted patents is that the test in the second domain is triggered based on the completion of the test in the first domain – once the first domain is done, the second domain then is activated." A20 at 6-9. Concluding that the operation of each domain under test must be separate and not overlapping, as the District Court does, however, does not mean the only way to achieve such independent operation is by an ***automatic clock triggering*** technique. This is especially true since no one disputes the use of a programmable capture window can effectuate the same separate and independent operation of the clock domains under test.

In the file history, the patentees point the Examiner to the prior art's requirement for certain clocks of different domains to be "aligned," meaning that the "all scan cells would be triggered simultaneously every few cycles" in response

to simultaneous clock pulses across all domains.[15] A322. "In contrast, [in] the present application . . . all second domain clock pulses can be placed in a staggered or in a sequential order." *Id.* The patentees provide the Examiner with a waveform diagram highlighting this distinction.



[15] The patentees acknowledged during prosecution that the prior art teaches an order sequence of certain clock pulses – as shown on the following diagram by the "s" pulses for the Nadeau-Dostie-2 waveform and the "c" pulses for the Hertherington waveform. A322. Unlike the patents-in-suit, which require all clock pulses in the capture window to be intentionally skewed, the patentees note that the prior art requires alignment – the "c" pulses of the Nadeau-Dostie-2 waveform and the "s" pulse of the Hertherington waveform. A322.

A325 (emphasis added). It is this distinction the patentees carry over to the specification: "[n]o prior art using multiple skewed capture clocks were proposed to test delay or stuck-at faults requiring two or more capture clocks for full or partial scan." A140 at 3:1-3. The patentees tell the Examiner that this differentiation allows "the present invention [to] eliminate [the unintended] clock skew problems" of the prior art. A323.

The District Court correctly points to the patentees' use of "triggering" when referring to the prior art requirement that certain clock pulses be triggered simultaneously. A19-20. In differentiating prior art, however, the patentees make no mention of how clock pulses are "placed in a staggered order or in a sequential order." A322. Neither law nor reason support the supposition that the patentees' mere use of the term triggering during prosecution in a different context constitutes "clear and unmistakable disavowal" of any method for the ordering of capture clocks other than automatic clock triggering. *Grober v. Mako Products, Inc.*, 686 F.3d 1335, 1341 (Fed. Cir. 2012) ("When a patentee makes a 'clear and unmistakable disavowal of scope during prosecution,' a claim's scope may be narrowed under the doctrine of prosecution disclaimer.")

Cisco's prosecution history argument focuses not upon what the patentees said, but on one figure in a provisional application that the patentees submitted as prior art later during the prosecution. A87. Cisco is correct, this figure, unlike the

waveform diagram provided to the Examiner, depicts a prior art use of the launch on capture technique for delay fault testing, as the activity of the scan enable signal depicts.

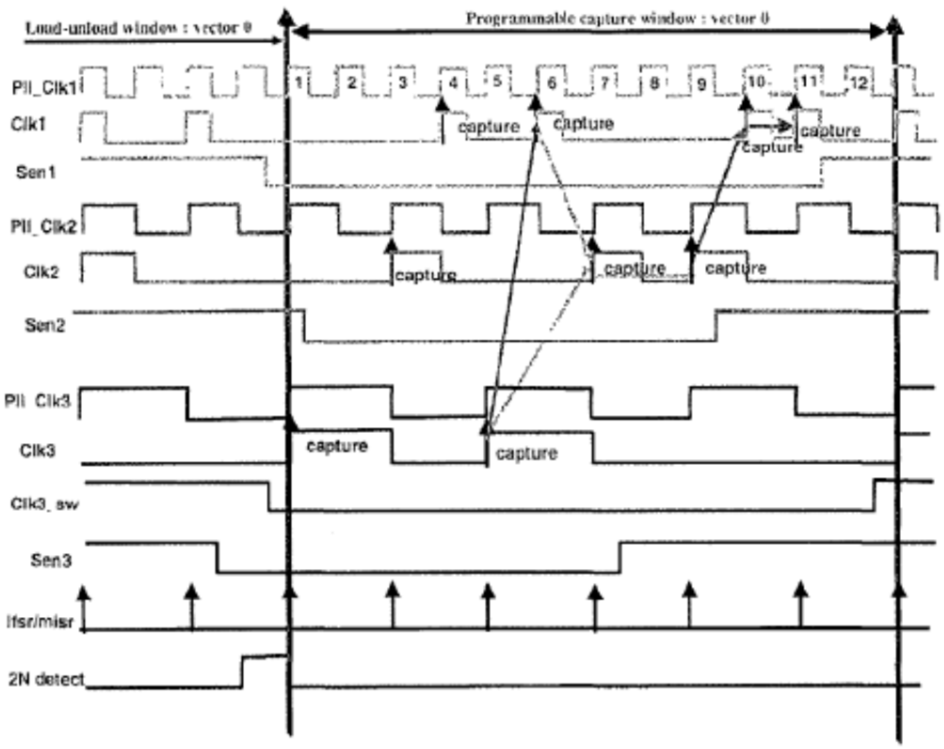


Fig. 12 :Extension of Scheme 2 to avoid invalid states and false paths.

A354. Cisco is also correct, the patentees during prosecution indicated their use of the launch on capture technique distinguished their invention from certain prior art. A322. According to Cisco's logic, in order to preserve validity, ordering by an automatic clock triggering method must be the invention because prior art disclosed the launch on capture technique using a programmable capture window.

Cisco's reasoning suffers numerous flaws. First, Cisco hides from this Court's "admonish[ment] against judicial rewriting of claims to preserve validity." *Rhine v. Casio, Inc.*, 183 F.3d 1342, 1345 (Fed. Cir. 1999). Second, Cisco's premise is false – what differentiates the claimed invention from prior art is not simply the invention's use of the launch on capture technique. As discussed above, use of the launch on capture technique may have been cited as a differentiating feature, but it is not the only, nor the overriding, feature the patentees emphasize as differentiating their invention from prior art. A140 at 3:1-4.

Finally, Cisco feebly argues that Figure 12 from this prior art reference shows an ordered sequence of capture clocks, a contention that collapses under the slightest scrutiny. **First**, as emphasized below, the figure fails to show an ordered sequence of capture clocks – there are overlapping clock pulses in all three of the clock domains, as shown in the following diagram by the red circles. A354. **Second**, while the figure depicts several inter-clock domain fault tests, it shows only a single intra-clock domain fault test, depicted by the horizontal arrow in clock domain 1, as emphasized by the blue square in the following diagram. As discussed above, the specifications claim an ordered sequence of capture clocks as easing difficulties associated with intra-domain delay fault testing at-speed, while acknowledging continued difficulties with inter-clock domain testing. A140 at 4:60-65. Figure 12 depicts the prior art method that seeks to achieve alignment,

which, if achieved, eases the difficulty associated with inter-domain fault testing. A338 ("The programmable capture window comprises of captures in different clock domains and some shift operations to create inter-domain at-speed capture."); A549 ("A programmable capture window allows capture in interacting domains to take place at different times to eliminate the clock skew problem.")

Third, and like all other prior art references, the technique disclosed requires the clocks for each domain have the same source and have frequencies that are the same or in a ratio with one another – *i.e.* be synchronous.[16] A337 ("Assumptions…[f]or every pair of different frequencies used in the design, one is a submultiple of the other.").

[16] As explained in this provisional application, despite the synchronous clocks, a skew still has developed along the scan enable signal. A347.

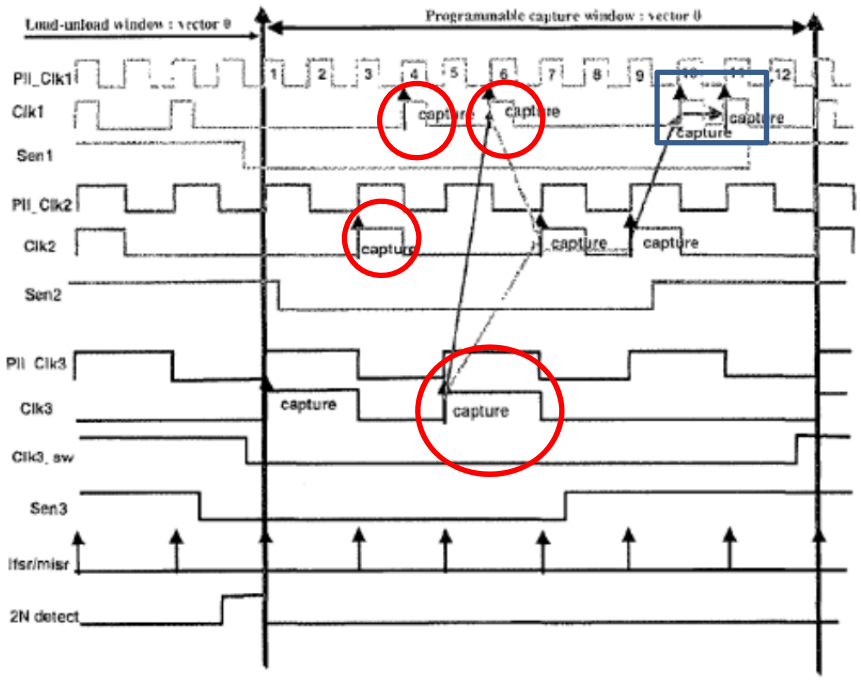


Fig. 12 :Extension of Scheme 2 to avoid invalid states and false paths.

A354 (emphasis added).

Cisco will obviously disagree, but whether this prior art reference anticipates or may help to render obvious one or all of the patents-in-suit is not before this Court at this time and is not an issue decided on claim construction.

C. Highlighting the Difficulties With Techniques Dependent Upon Alignment Does Not Disavow Ordering by Programming

Although not mentioned by the District Court, Cisco may argue, as it did below, for limiting the methods of "providing ordered capture clocks" to automatic clock triggering because the specification disparages other prior art methods. Cisco is correct that "'[w]here the specification makes clear that the invention does

not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent, even though the language of the claims, read without reference to the specification, might be considered broad enough to encompass the feature in question.'" *Chicago Bd. Options v. Intern. Securities Exchange*, 677 F.3d 1361, 1372 (Fed. Cir. 2012) (*quoting Honeywell Intern., Inc. v. ITT Industries, Inc.*, 452 F.3d 1312, 1319 (Fed. Cir. 2006) (further citation omitted). In *Chicago Bd.*, this Court states that the "repeated derogatory statement about [floor based trading] reasonably may be viewed as a disavowal of that subject matter from the scope of the Patent's claims." *Id.*

"Mere criticism of a particular embodiment encompassed in the plain meaning of a claim term is[, however,] not sufficient to rise to the level of clear disavowal." *Thorner*, 669 F.3d at 1366. Similarly, "a patentee's discussion of the shortcomings of certain techniques is not a disavowal of the use of those techniques in a manner consistent with the claimed invention." *Epistar Corp. v. Int'l Trade Comm'n*, 566 F.3d 1321, 1336 (Fed. Cir. 2009) (direct criticism of a particular technique did not rise to the level of clear disavowal); *Spine Solutions, Inc. v. Medtronic Sofamor Danek USA, Inc*. 620 F.3d 1305, 1315 (Fed. Cir. 2010) (even where a particular structure makes it "particularly difficult" to obtain certain benefits of the claimed invention, this does not rise to the level of disavowal of the structure).

Cisco will point to the specification's discussion of a method disclosed in a prior art publication Hetherington *et al.* (1999), which is reflected on the waveform diagram provided to the Examiner. The specification notes "[t]his approach rests on using multiple shift-followed-by-capture clocks each operating at its operating frequency, in a programmable capture window, to detect faults at-speed." A140 at 3:7-11. The specification identifies the problem of unintended clock skews with methods requiring alignment. "These shift clock pulses may also need precise timing alignment. As a result, it becomes quite difficult to perform at-speed self-test for designs containing clock domains operated at totally unrelated frequencies . . ." A140 at 3:14-18. Unlike the prior art, "the present invention does not require using shift clock pulses in the capture window, inserting capture-disabled logic in normal mode, applying clock suppression on capture clock pulses, and programming complex timing waveforms on scan enable (SE) signals." A140 at 3:26-30.

First, contrary to Cisco's argument to the District Court, this portion of the specification – the only portion Cisco cites on this point – does not disparage the use of a programmable capture window for triggering the clocks of different domains. Here, the specification distinguishes its order sequence method from prior art methods requiring alignment. Furthermore, even construing this language as criticism, "this criticism does not rise to the level of a disavowal. A disavowal

requires 'expression of manifest exclusion or restriction, representing a clear disavowal of claim scope.'" *Epistar Corp*., 566 F.3d at 1335 (quoting *Teleflex, Inc. v. Ficosa N. Am. Corp*., 299 F.3d 1313, 1325 (Fed. Cir. 2002).

II. THE DISTRICT COURT'S OWN REASONING FAILS TO SUPPORT READING IN THE LIMITATION "FROM THE CAPTURE CLOCK" INTO DISPUTE #8

The District Court construes the phrase "each shift clock pulse comprising a clock pulse applied in scan mode," Dispute #8, as "<u>each shift clock pulse comprising a pulse of the capture clock</u> at a frequency that need not be the same as the normal operating frequency of the domain's system clock." A32 (emphasis added). This phrase is found in independent claims 1 and 29 of the '213 patent and claim 1 of the '126 patent. The limitation that "each shift clock pulse" be a clock "pulse of the capture clock" allows Cisco to avoid infringement. According to Cisco, since the accused instrumentalities use distinct clocks derived from distinct sources to perform the separate shift and capture operations, no shift clock pulse is a clock "pulses of the capture clock." A5.

Neither the specification nor the prosecution history support importing the limitation that "each shift clock pulse compris[es] a pulse of the capture clock." Instead the specification and prosecution history both support the absence of any restriction on the clock that comprises the shift clock pulses, and suggest simply

eliminating the District Court's limitation from the construction –"each shift clock pulse comprising a pulse of ~~the capture~~ [a] clock at a frequency that need not be the same as the normal operating frequency of the domain's system clock."

The District Court's limitation on "shift clock pulses" to clock "pulses of the capture clock" curiously contradicts the reasoning offered to support the construction. The District Court rejects "Cisco['s] attempt[] to limit the clock that can generate this [shift] clock pulse to . . . the same clock generating the capture clock pulses . . . ." A32 at 13-15. According to the District Court, Cisco's "construction ignores the specification, which identifies the reach of the invention to embrace both self-test and scan-test." *Id.* at 16-17. In scan-test, an ATE generates the clock for at least the shift function, meaning that shift clock pulses are not pulses of the system clock. A141 at 5:52-60. The District Court "[a]dditionally, [notes] the specification recognizes that separate clocks can be responsible for shift clock pulses and capture clock pulses." A32 at 19-20, A141 at 5:28-32. Concluding, the District Court highlights, "Cisco['s] acknowledgement [that], while adequate delay fault testing requires capture clock pulses be at speed [which may necessitate the use a domain's system clock], 'the shifting frequency is irrelevant to at-speed testing.'" A32 at 20-21.

Similarly, the District Court's construction conflicts with his construction of Dispute #10. In this mean-plus-function construction, the District Court rejects

Cisco's effort to limit the structure for the function of shifting in data to the capture clock. A34. The District Court highlights that "the specification makes clear that the 'multiple-capture DFT system of the present invention further comprises any method or apparatus for performing the shift operation at any selected clock speed within each clock domain. The specification also recognizes that separate clocks can generate shift clock pulses and capture clock pulses." A5 (citations omitted).

It is difficult to reconcile the District Court's construction with his reasoning. By recognizing that shift clock pulses can come from different clock generation sources, the District Court necessarily recognizes that shift clock pulses need not comprise clock pulses of the system clock. Unlike the capture clock operation – which references the advantage of utilizing a domain's system clock for true at-speed delay fault testing[17] – the specifications indicate no need or desire that shift clock pulses comprise pulses of any particular clock or that the clock come from a particular source. A140 at 3:14-18, 26-30, 4:39-43, 48-49. In fact, Cisco cannot consistently argue that the specification's use of the phrase "present invention" can limit the invention to automatic clock triggering and at the same time argue that shift clock pulses must be construed as limited to clock pulses of the capture clock – "[t]he multiple-capture DFT system of the present invention further comprises any method or apparatus for executing the shift and compact or

[17] *See* A139 at 2:23-28, A141 at 5:54-60.

shift and compare operations concurrently during each self-test or scan-test cycle." A140 at 4:5-10.

The confusion between the District Court's construction and his reasoning likely stems from the construction of "capture clock." The District Court rejects Cisco's insertion of "capture clock" into its proposed construction as an effort to limit each shift clock to a pulse of "a reconfigured system clock." A32. This reasoning suggests that "capture clock" should not be construed here as a "reconfigured system clock."

Previously in his order, however, the District Court rejects SynTest's suggestion that capture clock be construed simply as a test clock, irrespective of clear evidence in the file history of the patentees, acting as their own lexicographer, intended such a construction. A21. Specifically, and responding to "the Examiner's concern that a capture clock should contain only capture clock pulses and a shift clock should contain only shift clock pulses," the patentees state they "happened to call the test clock 'the capture clock,' which inadvertently and unfortunately has created some confusion." A321; *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir.1996) ("[A] patentee may choose to be his own lexicographer and use terms in a manner other than their ordinary meaning, as long as the special definition of the term is clearly stated in the patent specification or file history.").

Rejecting a construction of "capture clock" as either a "reconfigured system clock" or a "test clock," leaves an ordinary meaning of "capture clock" – a clock signal made up of clock pulses used to drive the capture operation of a scan-test or a self-test. This ordinary meaning of capture clock, however, demonstrates the error of the District Court construction, which limits each shift pulse to "a pulse of the capture clock" – a construction that the file history shows makes no sense.

Cisco no doubt will point to language in the preamble of claims 1 and 29 of the '213 patent – "each capture clock comprising a selected number of shift clock pulses and a selected number of capture clock pulses" as well as similar language in claim 2.[18] A150 at 23:26-27, 52-54, A151 at 26:18-22. This language, however, predates the Office Action where "[t]he Examiner asserts that any clock is comprised of only pulses belonging to the particular clock and cannot be comprised of pulses belonging to any other clock. Hence a capture clock is comprised of only pulses belonging to the capture clock, *i.e.*, capture clock pulses, and cannot be comprised of shift clock pulses because shift clock pulses belong to a shift clock not a capture clock." A288. The Examiner then "points out that [he] does not believe that is what the [patentee] intends anyway." *Id.* In response to the Examiner's comment, the patentees changed the specific language in the body

[18] Claim 1 of the '126 patent does not include this or similar language in its preamble.

of claims 1 and 29 that caused the Examiner's concern, acknowledging the confusion caused by the "use of capture clock to refer to a test clock." A321. While Cisco may claim that the patentees failed to correct this ambiguity in the preamble, the District Court has already ruled the preambles of claims 1 and 29 are not limiting. A15-17.

Contrary to the specification and the District Court's reasoning, Cisco may finally attempt to use this language from the preamble to argue the same clock must control both the shift and capture function. At best this argument confuses the difference between a clock and its source. Obviously, clocks of different frequencies are different clocks irrespective of whether the clocks are generated from the same source. As the preamble makes clear, consistent with the body of the claim and the District Court's construction, the clock controlling the shift operation is distinct from the clock controlling the capture operation. Shift clock pulses are applied in scan mode and capture clock pulses are applied in normal mode, *i.e.,* at likely distinct frequencies– which means they are different clocks, as the District Court's construction correctly provides. A150 at 23:22-40.

Consistent with the specification, the file history, and the District Court's reasoning, the invention reaches shift clock pulses comprising a clock generated from sources other than the source of a domain's system clock and can be at frequencies different than the frequency of the clock controlling the capture

operation. The record fails the exacting standard necessary to show that the patentee "clearly" and "unmistakabl[y]" intended to limit "each capture clock pulse" to a clock "pulse of the capture clock." *Thorner*, 669 F.3d at 1365-1367.

III. "CAPTURE CLOCK" SHOULD NOT BE CONSTRUED AS LIMITED TO A "RECONFIGURED SYSTEM CLOCK" ONLY

The patents-in-suit claim as a feature the ability to utilize the clock that orders the function of a domain in normal operation – that domain's system clock – to control the capture operation, which allows for delay fault testing of each clock at-speed. A150 at 23:28-30, 24:59-64. Stating the obvious, when the system clock performs the capture operation it is the capture clock for the test operation, as indicated by the specification. The converse, however, is not true. The ability to use the system clock to perform the capture operation does not require all capture clocks be reconfigured system clocks, as the District Court's construction seems to conclude.

Cisco may first argue that SynTest waived any ability to challenge the construction of "capture clock" as anything but a "reconfigured system clock" by initially stipulating to such a construction. Consistent with this Court's requirements, SynTest clearly objected to "capture clock" being constructed to cover only "reconfigured system clocks," presented this objection and an alternative construction to the District Court, who clearly considered SynTest's

objection and alternative construction in his claim construction order. A22; *compare Regents of Univ. of Minnesota v. AGA Medical Corp*., 717 F. 3d 929, 946 (Fed. Cir. 2013) ("If the University objected to that construction, it should have presented its objection and its alternative construction to the district court."). The District Court does not simply adopt the parties' construction of capture clock as a reconfigured system clock, but finds that the specification supports the construction. A21.

Cisco cannot contend that the ordinary meaning of capture clock is a reconfigured system clock. To prevail that all "capture clocks" of the claimed invention are limited to "reconfigured system clocks," Cisco must demonstrate to an exacting standard that "the patentee set forth a definition of the disputed claim term other than its plain and ordinary meaning" and must "clearly express an intent to redefine the term." *Thorner*, 669 F.3d at 1365. While the specification clearly indicates that a "reconfigured system clock" can be a "capture clock," to limit all "capture clocks" to "reconfigured system clocks" also requires exacting proof from Cisco of the "[t]he patentee['s] intent to deviate from the ordinary and accustomed meaning of a claim term by including in the specification expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope." *Teleflex*, 299 F.3d at 1325; *Home Diagnostics, Inc. v. LifeScan, Inc*., 381 F.3d 1352, 1358

(Fed. Cir. 2004) ("Absent a clear disavowal in the specification or the prosecution history, the patentee is entitled to the full scope of its claim language.").

Without question the specification "propose[s] . . . tak[ing] over control of all system clocks and reconfigure[ing] them as capture clocks." A139 at 1:48-50. Certain drawings depict "all system clocks a[s] . . .reconfigur[ing] to operate at" a slower clock speed. A143 at 9:18-20. The specification then identifies these "reconfigured system clocks as capture clocks." *Id.* Using "reconfigured system clocks" to perform capture operations, however, are not identified – unlike the automatic triggering method discussed above – as a feature of the "present invention." Instead, the specification describes "the present invention [as] further compris[ing] any method or apparatus for allowing use of internally generated or externally-controlled capture clocks for at-speed scan-test or self-test." A141 at 5:57-60.

Curiously, the District Court reads this expansive language concerning the "capture clocks" as actually supporting the patentees' disclaimer of a capture clock being anything other than a reconfigured system clock. A22. The District Court cites the specification providing that "[a]n integrated circuit or circuit assembly, in general, contains two or more system clocks, each controlling one . . . clock domain. Each system clock is either directly coming from a primary input [access point to the circuit] or generated internally." A139 at 1:32-36. The District Court

simply conflates the source of the system clock during normal operation – which can come from a source on the ASIC itself or from another source on the device – and the ability of an ATE, external to both the device and the ASIC, to generate clocks for testing. A602 (discussing problems with use of derived clocks in testing). Any clock generated from a source other than its source during normal operations is simply not a system clock. While the District Court may reason that the claimed invention utilizes the same clock source regardless of whether self-test or scan-test is performed, the language, internally generated **or** externally controlled would need to read internally generated **and** externally controlled to support such logic.

The District Court further limits the meaning of "capture clocks" to "reconfigured system clocks . . . that contain both shift clock pulses and capture clock pulses, depending on the mode of operation." A22. This construction runs directly contrary to the District Court's later acknowledgement, as discussed above, that "the specification recognizes that separate clocks can be responsible for the shift clock pulses and capture clock pulses" and rejecting Cisco's attempt to "limit the clock that can generate this pulse [– the pulse of the shift clock –] to a reconfigured system clock." A32. In this context, the District Court recognized the distinction between a capture clock generated internally and a shift clock pulse

controlled externally – Cisco's "construction ignores the specification, which identifies the reach of the invention to embrace both self-test and scan-test." *Id.*

The District Court's construction seems to conflict with his mean-plus-function construction in Dispute #10. With respect to Dispute #10, the District Court explicitly rejected Cisco's effort to limit the disclosed structure to "the capture clock," because such a construction would "inappropriate[ly]" "read out scan-test" from the invention. A35. If a capture clock must always be a reconfigured system clock, then an ATE could never be the source of the capture clock, which would "read out scan-test" from the invention.

Nothing in the file history supports limiting all capture clocks claimed within the invention to reconfigured system clocks. As discussed above, the Examiner expressly rejected claim language indicating that the capture clock could contain both shift clock pulses and capture clock pulses. A288. The patentees did not respond that they had defined a capture clock as a reconfigured system clock that could contain either shift clock pulses or capture clock pulses depending on operating mode. A320-321. Instead, the patentees sought to eliminate the Examiner's concerns by amending claim language to reflect that different clocks would control depending on the mode – during shift the frequency would be in scan mode and during capture the frequency would be in normal mode – *i.e.* two distinct clocks. A309. The patentees then apologized for the confusion

attributable to their decision to "call the test clock the 'capture clock.'" A321. The patentees acknowledged that, "[i]n many designs, a clock domain may be only controlled by one test clock. Thus, this test clock will contain clock pulses applied in scan mode (hence shift clock pulses) and clock pulses in normal mode (hence capture clock pulses)." *Id.* The patentees, however, in no way indicate any intent, let alone an unmistakable, clear intent, to limit their invention to self-test designs where a clock domain is controlled by only one test clock.

If anything, the patentees show a clear intent to act as their own lexicographers and redefine "capture clock" as a "test clock." Alternatively, this Court could find that neither Cisco nor SynTest offer sufficient proof to support redefining "capture clock" to reach beyond its ordinary meaning – a clock containing capture clock pulses.

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CONCLUSION

For the foregoing reasons, SynTest respectfully requests that this Court reverse the judgment below due to error in the District Court's claim construction. SynTest further requests that this Court find that the District Court erred by reading limitations into the ordinary meaning of certain claim language that failed to meet the exacting standard necessary for such action.

DATED: August 22, 2014

Respectfully Submitted,

s/ John Shaeffer

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SYNTEST TECHNOLOGIES, INC.

ADDENDUM

Appendix No	Docket No.	Document
A1-A7	**84**	**JUDGMENT**
A8-36	**83**	**CLAIM CONSTRUCTION ORDER**
A113-151	**45-1**	**US PATENT 7,007,213,**
A153-191	**45-2**	**US PATENT 7,434,126**
A193-231	**45-3**	**US PATENT 7,779,323**

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

SYNTEST TECHNOLOGIES, INC., Plaintiff, v. CISCO SYSTEMS, INC., Defendant.	Case No. 5:12-cv-05965-PSG **JUDGMENT** **(Re: Docket Nos. 74, 78 and 83)**

Earlier this week the court issued a more fulsome claims construction order spelling out the rationale for the constructions issued in this case.[1] The court now reenters the attached stipulated judgment of non-infringement in favor of Defendant Cisco Systems, Inc. and against Plaintiff SynTest Tecnologies, Inc.[2] The case thus is passed to the circuit court to consider any appropriate appeal. The Clerk shall close the file.

IT IS SO ORDERED.

Dated: June 12, 2014

PAUL S. GREWAL
United States Magistrate Judge

[1] *See* Docket Nos. 74 and 83.

[2] *See* Docket No. 78.

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CISCO SYSTEMS, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SYNTEST TECHNOLOGIES, INC., Plaintiff, v. CISCO SYSTEMS, INC., Defendant.	Case No. 5:12-cv-05965-PSG **[~~PROPOSED~~] STIPULATED JUDGMENT OF NON-INFRINGEMENT**
CISCO SYSTEMS, INC., Counterclaim-Plaintiff, v. SYNTEST TECHNOLOGIES, INC., Counterclaim-Defendant.	Hon. Judge Paul S. Grewal

Plaintiff SynTest Technologies, Inc. ("SynTest") and Defendant Cisco Systems, Inc. ("Cisco"), by and through their undersigned counsel, hereby agree and stipulate as follows:

Whereas,

1. On November 21, 2012, SynTest filed a complaint against Cisco alleging infringement of U.S. Patent Nos. 7,007,213, 7,434,126 and 7,779,323 (collectively the "Asserted Patents"), and the case was assigned to the Honorable Paul S. Grewal;
2. On January 16, 2013, Cisco filed its answer and counterclaims alleging, among other things, its non-infringement of the Asserted Patents and seeking from this Court a declaration to that effect;
3. Consistent with this Court's schedule, on August 16, 2013, both Cisco and SynTest filed with the Court their respective Opening Claim Construction Briefs and followed thereon with additional claim construction briefing;
4. On October 18, 2013, this Court held a tutorial on the relevant technology and a hearing on claim construction ("Claim Construction Hearing");
5. During the course of the Claim Construction Hearing counsel for both SynTest and Cisco agreed that the construction of multiple terms could be case dispositive;

NONINFRINGEMENT BASIS NO. 1:

6. This Court construed certain claim terms in the Asserted Patents in its Claim Construction Order Dated October 22, 2013 (ECF No. 74) ("Claim Construction Order") as will be explained in the Court's subsequent Memorandum Opinion;
7. The Court construed the claim limitation "providing ordered capture clocks" in Claim 1 of the '126 Patent as "triggering a capture clock pulse in at least one clock domain in response to a capture clock pulse in another clock domain";
8. The Court construed the claim limitation "applying an ordered sequence of capture clock pulses to all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture clock pulses comprising at least two capture clock pulses from two or more selected capture clocks, for

controlling two or more clock domains, in a sequential order" in Claims 1 and 29 of the '213 Patent as "applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode by triggering a capture clock pulse in the latter clock domain in response to a capture clock pulse in the former clock domain";

9. The Court construed the claim limitation "applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least a plurality of capture clock pulses from two or more selected capture clocks placed in a sequential order such that all clock domains are never triggered simultaneously during a capture operation" in Claim 1 of the '323 Patent as "applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode by triggering a capture clock pulse in the latter clock domain in response to a capture clock pulse in the former clock domain such that all clock domains are never triggered simultaneously during a capture operation";

10. Cisco asserts that the Cisco Accused Instrumentalities[1] do not practice the limitations recited above in Paragraphs 7-9 as construed by the Court at least because they trigger a domain's capture clock pulses based on the number of cycles

[1] As used herein, "Cisco Accused Instrumentalities" refers to all instrumentalities made, used, sold, or offered for sale by or for Cisco that are alleged to directly or indirectly infringe one or more claims of any of the Asserted Patents, including at least the devices and/or services referred to in SynTest's Patent L.R. 3-1 contentions.

that have occurred in a common reference clock, rather than triggering a capture clock pulse in at least one clock domain in response to a capture clock pulse in another clock domain, and, therefore, a final judgment of noninfringement should be entered in Cisco's favor.

11. Cisco has indicated that it intends to seek summary judgment in this action on at least the grounds described in the preceding paragraph, and the parties agree that the Court's Claim Construction Order would warrant summary judgment of noninfringement at this time on that basis and, therefore, a final judgment of noninfringement should be entered in Cisco's favor;

NONINFRINGEMENT BASIS NO. 2:

12. The Court construed each of the phrases "each shift clock pulse comprising a clock pulse applied in scan mode" and "each capture clock pulse comprising a clock pulse in normal mode," in Claim 1 of the '126 Patent and Claims 1 and 29 of the '213 Patent as referring to "a pulse of the capture clock";
13. Cisco asserts that the clock that comprises capture clock pulses in the Cisco Accused Instrumentalities does not also comprise shift clock pulses and, therefore the Cisco Accused Instrumentalities lack a shift clock pulse that comprises a pulse of the capture clock and do not practice this limitation as construed by the Court;
14. Cisco has indicated that it intends to seek summary judgment in this action on at least the grounds described in the preceding paragraph, and the parties agree that the Court's Claim Construction Order would warrant summary judgment of noninfringement at this time on that basis and, therefore, a judgment of noninfringement should be entered in Cisco's favor on all claims of infringement of the '213 and the '126 Patent; and
15. SynTest intends to appeal the Court's Claim Construction Order to the Federal Circuit.

STIPULATION RE: NON-INFRINGEMENT IN LIGHT OF CLAIM CONSTRUCTION RULING

Therefore:

16. To promote judicial efficiency and avoid the waste of this Court's and the parties' resources, under the Court's claim constructions as detailed above, SynTest and Cisco stipulate to entry of final judgment of noninfringement in Cisco's favor on SynTest's infringement claims.

17. FINAL JUDGMENT IS HEREBY ENTERED against SynTest and for Cisco on all claims asserted in SynTest's Complaint. SynTest shall take nothing against Cisco. FINAL JUDGMENT IS HEREBY ENTERED for Cisco and against SynTest on Cisco's counterclaim for declaratory judgment of non-infringement of the Asserted Patents.

18. Cisco's remaining counterclaims are dismissed without prejudice.

19. This is a final and appealable judgment.

20. In the event that this matter is remanded following an appeal, SynTest and Cisco agree that each party has not waived, but instead has reserved and may assert, all of their rights, claims, arguments and defenses, including but not limited to Cisco's defenses and counterclaims of noninfringement and invalidity.

21. Any deadline for seeking an order from the Court for an award of attorneys' fees or costs, including pursuant to 35 U.S.C. § 285, will not begin to run until issuance of the mandate following any appeal from this Judgment.

So Stipulated on November 13, 2013

BAKER & BOTTS, LLP

By: /s/ Douglas M. Kubehl
Douglas M. Kubehl
Attorneys for Defendant Cisco Systems Inc.

LATHROP & GAGE LLP

By: /s/ John Shaeffer
John Shaeffer
Attorneys for Plaintiff SynTest Technologies, Inc.

The Court having considered the above and finding good cause, the foregoing is **SO ORDERED** this 18th day of November 2013.

PAUL S. GREWAL
United States Magistrate Judge

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

SYNTEST TECHNOLOGIES, INC., Plaintiff, v. CISCO SYSTEMS, INC., Defendant.	Case No. 5:12-cv-05965-PSG **CLAIMS CONSTRUCTION ORDER** **(Re: Docket No. 74)**

In this patent infringement suit, Plaintiff SynTest Technologies, Inc. alleges that Defendant Cisco Systems, Inc. infringes U.S. Patent Nos. 7,007,213, 7,434,126 and 7,779,323. The parties submitted ten claim construction disputes from those asserted patents for resolution by the court. The court issued a summary construction order a few days after the hearing and explained that a more complete order would follow providing the court's reasoning.[1] The court now provides that reasoning.

[1] *See* Docket No. 74.

Case5:12-cv-05965-PSG Document78 Filed08/01/14 Page

I. BACKGROUND

A. The Parties

SynTest and Cisco are California corporations with principal places of business in this district.[2] SynTest creates and licenses tools for the design of application specific integrated circuits ("ASICs"). SynTest is the assignee of each of the asserted patents. Cisco is a former SynTest customer. SynTest alleges Cisco developed and uses ASICs practicing the patents-in-suit without a valid license.[3]

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[2] *See* Docket No. 64 at ¶¶ 4-5. The background material describing the technology at issue in this section is drawn from the parties' opening claim construction briefs. *See* Docket No. 44 at 1-6 and Docket No. 46 at 1-9.

[3] After the court issued its constructions, the parties stipulated that under those constructions Cisco's accused instrumentalities do not practice certain limitations and thus does not infringe the asserted patents. *See* Docket No. 78 at ¶¶ 7-14.

<u>NONINFRINGEMENT BASIS NO. 1:</u>

7. The Court construed the claim limitation "providing ordered capture clocks" in Claim 1 of the '126 Patent as "triggering a capture clock pulse in at least one clock domain in response to a capture clock pulse in another clock domain";

8. The Court construed the claim limitation "applying an ordered sequence of capture clock pulses to all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture clock pulses comprising at least two capture clock pulses from two or more selected capture clocks, for controlling two or more clock domains, in a sequential order" in Claims 1 and 29 of the '213 Patent as "applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode by triggering a capture clock pulse in the latter clock domain in response to a capture clock pulse in the former clock domain";

9. The Court construed the claim limitation "applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least a plurality of capture clock pulses from two or more selected capture clocks placed in a sequential order such that all clock domains are never triggered simultaneously during a capture operation" in Claim 1 of the '323 Patent as "applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode by triggering a capture clock pulse in the latter clock domain in response to a capture clock pulse in the former clock domain such that all clock domains are never triggered simultaneously during a capture operation";

10. Cisco asserts that the Cisco Accused Instrumentalities1 do not practice the limitations recited above in Paragraphs 7-9 as construed by the Court at least because they trigger a domain's capture clock pulses based on the number of cycles that have occurred in a

B. The Technology

1. Fault Testing the Logic of an Integrated Circuit

Before an ASIC can be manufactured, its logic must first be tested to see if it works as intended. Testing tools can be built into an AISC that work either with external automatic test equipment or alone. Testing tools built into the circuit itself are collectively known as a Built-In Self-Test.

ASICs commonly contain millions of "flip-flops" that act as memory cells. A flip-flop stores states of logic as a one or zero. The state of a flip-flop is controlled by electronic pulses that run through the ASIC. The frequency of these pulses is in turn controlled by a clock. The area of an ASIC controlled by a clock is called a clock domain. A single ASIC can have dozens of such domains – each controlled by separate clocks operating at different frequencies.

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common reference clock, rather than triggering a capture clock pulse in at least one clock domain in response to a capture clock pulse in another clock domain, and, therefore, a final judgment of noninfringement should be entered in Cisco's favor.

11. Cisco has indicated that it intends to seek summary judgment in this action on at least the grounds described in the preceding paragraph, and the parties agree that the Court's Claim Construction Order would warrant summary judgment of noninfringement at this time on that basis and, therefore, a final judgment of noninfringement should be entered in Cisco's favor;

NONINFRINGEMENT BASIS NO. 2:

12. The Court construed each of the phrases "each shift clock pulse comprising a clock pulse applied in scan mode" and "each capture clock pulse comprising a clock pulse in normal mode," in Claim 1 of the '126 Patent and Claims 1 and 29 of the '213 Patent as referring to "a pulse of the capture clock";

13. Cisco asserts that the clock that comprises capture clock pulses in the Cisco Accused Instrumentalities does not also comprise shift clock pulses and, therefore the Cisco Accused Instrumentalities lack a shift clock pulse that comprises a pulse of the capture clock and do not practice this limitation as construed by the Court;

14. Cisco has indicated that it intends to seek summary judgment in this action on at least the grounds described in the preceding paragraph, and the parties agree that the Court's Claim Construction Order would warrant summary judgment of noninfringement at this time on that basis and, therefore, a judgment of noninfringement should be entered in Cisco's favor on all claims of infringement of the '213 and the '126 Patent . . .

See also Docket No. 74.

2. Design For Test Techniques

Logic faults include "stuck-at" faults and "delay" faults. With a stuck-at fault, the state of the flip-flop is stuck at one or zero. A delay fault is one that causes the ASIC to operate slower than expected. The three patents in this case share a common specification and are directed to a specific design for test ("DFT") technique for detecting whether the logic in an ASIC suffers from any other type of fault. The asserted patents describe DFT techniques "that can facilitate detection or location of physical defects that can manifest themselves as logic faults within an integrated circuit or circuit assembly."[4]

The particular scan design at issue in the asserted patents involves loading (or "shifting") test patterns into storage elements of an ASIC using clock pulses known as "shift clock pulses."[5] When an ASIC receives the shift clock pulses and is operating in what is called "scan mode," the ASIC reacts by shifting the test stimuli into the ASIC's storage elements. Next, when the ASIC is operating in what is called "normal mode" and receives "capture clock pulses,"[6] those pulses cause the ASIC to operate on the loaded test stimuli as it would when operating in its normal functional mode.[7] Finally, when the ASIC is returned to scan mode and it receives additional shift clock

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[4] Docket No. 45-4, Ex. D at 5.

[5] Docket No. 45-1, Ex. A at Fig. 10.

[6] ASICs with multiple system clocks can experience "clock skew" among the system clocks, which can create difficulties in detecting faults. Docket No. 45-1, Ex. A at 1:39-47. One prior art approach to solving that problem involved taking "over control of all system clocks" and reconfiguring "them as capture clocks." *Id.* at 1:49-50. The parties agree that a "capture clock" is a "reconfigured system clock." *See* Docket No. 35, Ex. A, at 1; *see also* Docket No. 45-1, Ex. A at 9:20 ("The reconfigured system clocks are called capture clocks."). The particular type of "capture clock" claimed in the patents-in-suit is a single reconfigured system clock that provides both shift clock pulses and capture clock pulses – depending on the "mode" in which the circuit operates.

[7] In the "daisy-chain" technique, one variant of this general technique, the capture clock pulse of one domain is triggered by the occurrence of a capture clock pulse of a preceding domain. *See id.* at 4:66-5:10. The "token ring" technique, another variant, is similar, except that the second domain's capture clock pulse is triggered based by occurrence of a particular signal level in the preceding domain's capture clock pulses. *See id.* at 5:11-16. For both variants, the first capture clock pulse of one of the clock domains is triggered by activity of the capture clock pulse of the preceding clock domain.

pulses, the shift clock pulses are applied to collect or "shift out" of the storage elements the results of the circuit's operation, so that they can be analyzed.

3. Detecting Faults Within and Crossing Clock Domains

An "integrated circuit or circuit assembly, in general, contains two or more system clocks, each controlling one module, or logic block, called [a] clock domain."[8] In other words, a "clock domain" is a module or logic block of an ASIC that is controlled by a single system clock. The system clock is the clock that drives the normal functional operation of the clock domain. ASICs can experience logic faults that occur completely "within" a given clock domain, as well as faults that "cross" multiple clock domains.[9] One aspect of the invention claimed in the asserted patents is the ability to detect both faults within and faults crossing any two clock domains.[10]

C. The Independent Asserted Claims

1. Claim 1 of the '213 Patent

Independent claim 1 of the '213 patent provides:

1. A method for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly during self-test, where N>I, each clock domain having one or more capture clocks and one or more scan cells, each capture clock comprising a selected number of shift clock pulses and a selected number of capture clock pulses, each shift clock pulse comprising a clock pulse applied in scan mode, each capture clock pulse comprising a clock pulse applied in normal mode; said method comprising the steps of:

(a) generating and loading N pseudorandum stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly, by applying said shift clock pulses to all said scan cells in said scan mode for loading or shifting-in said N pseudorandom stimuli to all said scan cells, during a shift operation;

(b) applying an ordered sequence of capture clock pulses to all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture clock pulses comprising at least two capture clock pulses from two or more selected capture clocks, for controlling two or more clock domains, in a sequential order, wherein each said selected capture clock must contain at least one said capture clock pulse, and when detecting or locating selected delay faults within a clock domain, said selected

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[8] *Id.* at 1:31-33.

[9] *Id.* at 1:39-46.

[10] *See, e.g.*, *id.* at 1:16-18 ("[T]he present invention relates to the detection or location of logic faults within each clock domain and logic faults crossing any two clock domains, during self-test or scan-test, in an integrated circuit or circuit assembly.").

capture clock controlling the clock domain contains at least two consecutive said capture clock pulses to launch the transition and capture the output response; and

(c) compacting N output responses of all said scan cells to signatures, by applying said shift clock pulses to all said scan cells in said scan mode for compacting or shifting-out said N output responses to form said signatures, during a compact operation.[11]

2. Claim 1 of the '126 Patent

Independent claim 1 of the '126 patent provides:

1. A computer-aided design (CAD) method for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in scan-test and selftest mode, where N>1, each clock domain having one capture clock and a plurality of scan cells, each capture clock comprising a selected number of shift clock pulses and a selected number of capture clock pulses, each shift clock pulse comprising a clock pulse applied in scan mode, each capture clock pulse comprising a clock pulse applied in normal mode, said CAD method comprising the computer-implemented steps of:

(a) compiling the HDL code or netlist that represents said integrated circuit or circuit assembly in physical form into a design database;

(b) performing test rule check for checking whether said design database contains any multiple-capture rule violations in said scan-test or said self-test mode;

(c) performing test rule repair until all said multiple-capture rule violations have been fixed;

(d) performing multiple-capture test synthesis for generating a testable HDL code or netlist; and

(e) generating HDL test benches and automatic test equipment (ATE) test programs for verifying the correctness of said testable HDL netlist in said scan-test or said self-test mode.[12]

3. Claim 1 of the '323 Patent

Independent claim 1 of the '323 patent provides:

1. An apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in scan-test or self-test mode, where N>1, each clock domain having one capture clock and a plurality of scan cells, each capture clock comprising a plurality of capture clock pulses; said apparatus comprising:

(a) means for generating and shifting-in N test stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during a shift-in operation;

(b) means for applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least a plurality of capture clock pulses from two or more selected capture clocks placed in a sequential order such that all clock domains are never triggered simultaneously during a capture operation; and

(c) means for analyzing output responses of all said scan cells to locate any faults therein.[13]

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[11] *See* Docket No. 45-1 at 23:10-46.

[12] *See* Docket No. 45-2 at 22:39-64.

II. LEGAL STANDARDS

Almost nine years after the Federal Circuit's seminal *Phillips* decision,[14] the canons of claim construction are now well-known – if not perfectly understood – by parties and courts alike. "To construe a claim term, the trial court must determine the meaning of any disputed words from the perspective of one of ordinary skill in the pertinent art at the time of filing."[15] This requires a careful review of the intrinsic record, comprised of the claim terms, written description, and prosecution history of the patent.[16] While claim terms "are generally given their ordinary and customary meaning," the claims themselves and the context in which the terms appear "provide substantial guidance as to the meaning of particular claim terms." Indeed, a patent's specification "is always highly relevant to the claim construction analysis."[17] Claims "must be read in view of the specification, of which they are part."[18] Although the patent's prosecution history "lacks the clarity of the specification and thus is less useful for claim construction purposes," it "can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be."[19] The court also has the discretion to consider extrinsic evidence, including dictionaries, learned treatises, and testimony from experts and

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[13] *See* Docket No. 45-3 at 22:39-58.

[14] *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005).

[15] *Chamberlain Group, Inc. v. Lear Corp.*, 516 F.3d 1331, 1335 (Fed. Cir. 2008).

[16] *See id.* ("To construe a claim term, the trial court must determine the meaning of any disputed words from the perspective of one of ordinary skill in the pertinent art at the time of filing. Intrinsic evidence, that is the claims, written description, and the prosecution history of the patent, is a more reliable guide to the meaning of a claim term than are extrinsic sources like technical dictionaries, treatises, and expert testimony.") (citing *Phillips*, 415 F.3d at 1312).

[17] *Phillips*, 415 F.3d at 1312-15.

[18] *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995); *see also Ultimax Cement Mfg. Corp v. CTS Cement Mfg. Corp.*, 587 F. 3d 1339, 1347 (Fed. Cir. 2009).

[19] *Phillips*, 415 F.3d at 1317 (internal quotations omitted).

inventors.[20] Such evidence, however, is "less significant than the intrinsic record in determining the legally operative meaning of claim language."[21]

III. DISCUSSION

A. Dispute #1: Whether the Preamble to Claim 1 of the '126 Patent is Limiting

CLAIM TERM/DISPUTE #1	
Whether the claim preambles of independent claims 1 and 29 of the '213 patent, claim 1 of the '126 patent and claim 1 of the '323 patent are limiting.	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
Not a claim construction issue	The preambles are limiting
CONSTRUCTION/RESOLUTION	
Only the preamble to claim 1 of the '126 patent is limiting.	

The parties dispute whether the claim preambles are limiting with respect to the '213 patent (claims 1 and 29), the '126 patent (claim 1) and the '323 patent (claim 1).

Although SynTest believes the question does not constitute a claim construction issue, it argues in the alternative that not all of the preambles are limiting. Because language in the preambles is repeated in the claim terms or referenced elsewhere in the patent, many of the ideas in the preambles necessarily will be addressed in other portions of the construction and there is no reason for the court to construe them within the preamble. SynTest does recognize one exception: the preamble to claim 1 of the '126 patent. The reason is that limitations A through E of that claim merely describe performing tasks on a circuit and limitations from the preamble are necessary for these later limitations to have meaning.[22] In contrast, claims 1 and 29 of the '213 patent fully

[20] *See id.* ("Although we have emphasized the importance of intrinsic evidence in claim construction, we have also authorized district courts to rely on extrinsic evidence, which 'consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises.'") (quoting *Markman*, 52 F.3d at 980).

[21] *Id.* (citing *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 862 (Fed. Cir. 2004)) (internal quotations and additional citations omitted).

[22] *See* Docket No. 45-2, Ex. B at 22:39-64.

describe the concept of testing within step B: the claim preamble is merely extolling the virtues of the patent and, according to SynTest, is not necessary to provide structure to the claim.[23] Similarly, the preamble from claim 1 of the '323 patent is not limiting, according to SynTest, because the purported limitation that N be greater than one is fully described in step B of claim 1.

Cisco disagrees, relying upon the Federal Circuit teaching that when "limitations in the body of the claim rely upon and derive antecedent basis from the preamble, then the preamble may act as a necessary component of the claimed invention."[24] According to Cisco, because all three preambles here supply antecedent bases for limitations that follow, all three claim preambles are limiting.

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[23] *See Deere & Co. v. Bush Hog, LLC*, 703 F.3d 1349, 1358 (Fed. Cir. 2012) (If "the body of the claim describes a structurally complete invention, a preamble is not limiting where it 'merely gives a name' to the invention, extols its features or benefits, or describes a use for the invention." (quoting *Catalina Marketing, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 809 (Fed. Cir. 2002))).

[24] *Eaton Corp. v. Rockwell Int'l Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003) ("The method steps of claim 14 thus require the manipulation of particular structures that are identified and described only by the preamble, during a particular sequence of events defined only" and therefore "the preamble of claim 14 limits the claimed invention."); *see also Electro Sci. Indus. v. Dynamic Details, Inc.*, 307 F.3d 1343, 1348 (Fed. Cir. 2002)

> To determine the meaning of "circuit boards," this court begins with the claim language. The preamble defines "circuit boards" as "at least first and second substantially identical circuit boards each having at least a first conductor layer, a dielectric layer, and a second conductor layer." References throughout the rest of the claim to "circuit boards" rely upon and derive antecedent basis from this preamble language. Therefore, this preamble definition limits the term "circuit boards" throughout the claim.

see also Rapoport v. Dement, 254 F.3d 1053, 1059 (Fed. Cir. 2001)

> First, we note that the disputed phrase "treatment of sleep apneas" is technically part of the preamble of the interference count, because it appears before the transition word "comprising." However, there is no dispute in this case that the phrase should be treated as a claim limitation. Moreover, without treating the phrase "treatment of sleep apneas" as a claim limitation, the phrase "to a patient in need of such treatment" would not have a proper antecedent basis.

see also Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1306 (Fed. Cir. 1999);

> The preamble statement that the patent claims a method of or apparatus for "producing on a photoreceptor an image of generated shapes made up of spots" is not merely a statement describing the invention's intended field of use. Instead, that statement is intimately meshed with the ensuing language in the claim. For example, both independent claims conclude with the clause "whereby the appearance of smoothed edges are given to the generated shapes". Because this is the first appearance in the claim body of the term "generated shapes", the term can only be understood in the context of the preamble statement "producing on a photoreceptor an image of generated shapes made up of spots."

SynTest has the better of the argument, at least on the merits. The determination of whether preambles are limiting necessarily affects the meaning – and therefore the size and scope – of the asserted claims.[25] Absent guidance on whether the preambles limit the scope of asserted claims, the jury would be invited "to choose between alternative meanings" of the disputed claims generating *O2 Micro* error. This court thus must resolve this "actual dispute regarding the proper scope" of the claims.[26] Because the body of claims 1 and 29 of the '123 patent as well as claim 1 of the '323 patent "describe a structurally complete invention,"[27] the preambles to those claims do not limit the meaning of the claims. A careful review shows the disputed language in the preambles as to those claims is repeated in the body of the claim and Cisco identifies no instance in which these preambles provide a unique description of structure referenced later in the claims. In short, there are no necessary antecedent bases in these preambles. In contrast, because the preamble to claim 1 of the '126 patent is necessary for limitations A through E to have meaning, that preamble is limiting.

[25] *See Laboratoires Perouse, S.A.S. v. W.L. Gore & Associates, Inc.*, 528 F. Supp. 2d 362, 372 (S.D.N.Y. 2007) ("The preamble is an introductory phrase that may summarize the invention, its relation to the prior art, or its intended use or properties," but may in some cases constitute a limitation.") (quoting 3-8 Chisum on Patents § 8.06 (2007)).

[26] *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1360 (Fed. Cir. 2008) ("When the parties raise an actual dispute regarding the proper scope of these claims, the court, not the jury, must resolve that dispute.").

[27] *See supra* note 23.

B. Dispute #2: " Providing Ordered Capture Clocks"

CLAIM TERM/DISPUTE #2	
"providing ordered capture clocks" The '213 patent (claims 1 and 29), the '126 patent (claim 1) and the '323 patent (claim 1)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
"providing two or more test clocks in a given order"	"triggering at least one clock domain's capture clock pulse in response to activity of another clock domain's capture clock pulse"
CONSTRUCTION/RESOLUTION	
"triggering a capture clock pulse in at least one clock domain in response to a capture clock pulse in another clock domain"	

Two disputes lie between the parties over the construction of "providing ordered capture clocks": (1) whether triggering should be incorporated into the construction and (2) whether a capture clock should be defined as a test clock.

1. Triggering Should Be Incorporated Into the Construction

The asserted patents specifically describe the "invention"[28] as using either "daisy-chain clock triggering" or "token-ring clock enabling" techniques for providing or applying ordered capture clocks:

> In the present invention, the multiple-capture DFT system uses a daisy-chain clock-triggering or token-ring clock-enabling technique to generate and order capture clocks one after the other.[29]
>
> * * *
>
> The multiple-capture DFT system in the present invention further comprises applying an ordered sequence of capture clocks and operating each capture clock at its selected clock speed in the capture operation (cycle). The ordered sequence of capture clocks is applied to

[28] *See Trading Techs. Int'l, Inc. v. eSpeed, Inc.*, 595 F.3d 1340, 1353-54 (Fed. Cir. 2010) (limiting claim by characteristic identified as the "present invention" in the specification, but cautioning against the risk of improperly reading a "preferred embodiment into" the claim) (citing *Saunders Group, Inc. v. Comfortrac, Inc.*, 492 F.3d 1326, 1332 (Fed. Cir. 2007) ("A patent that describes only a single embodiment is not necessarily limited to that embodiment.")); *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1117 (Fed. Cir. 2004) ("And, even where a patent describes only a single embodiment, claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction." (internal quotations and citations omitted)).

[29] Docket No. 45-1, Ex. A at 4:57-60.

the circuit under test one-by-one using the daisy-chain clock-triggering or token ring clock-enabling technique.[30]

Both techniques require generation of capture clock pulses for one clock domain in direct response to a capture clock pulse in another clock domain. For example, in the daisy-chain technique, the occurrence of a transition (e.g., from low-to-high or high-to-low) of a preceding clock domain's capture clock pulse triggers generation of capture clock pulses in the next clock domain.[31] The token-ring technique is similar, except that the next domain's capture clock pulses are activated based on the occurrence of a particular signal level (e.g. low or high) in the preceding domain's capture clock pulses.[32] In other words, daisy-chain clock-triggering "uses clock edges to trigger the next operation" and token-ring clock-enabling "uses signal levels to enable the next operation."[33] For both options, the occurrence of the first capture clock pulse of one of the clock domains depends directly on the activity of a capture clock pulse of a previous clock domain.

The term "triggering" encompasses the response requirement because the applicants specifically used the term "triggered" to describe how the claimed invention provided ordered

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[30] *Id.* at 5:34-40.

[31] *See* Docket No. 45-1, Ex. A at 4:66-5:10.

> As an example, assume that the capture cycle contains 4 capture clocks, CK1, CK2, CK3, and CK4. (Please refer to FIGS. 3 and 10 in the DETAILED DESCRIPTION OF THE DRAWINGS section for further descriptions). The daisy-chain clock-triggering technique implies that completion of the shift cycle triggers the GSE signal to switch from shift to capture cycle which in turn triggers CK1, the rising edge of the last CKI pulse triggers CK2, the rising edge of the last CK2 pulse triggers CK3, and the rising edge of the last CK3 pulse triggers CK4. Finally, the rising edge of the last CK4 pulse triggers the GSE signal to switch from capture to shift cycle.

Id. at 5:18-20.

> The only difference between these two techniques is that the former uses clock edges to trigger the next operation, the latter uses signal levels to enable the next operation.

[32] *See id.* at 5:11-16

> The token-ring clock-enabling technique implies that completion of the shift cycle enables the GSE signal to switch from shift to capture cycle which in turn enables CK1, completion of CKI pulses enables CK2, completion of CK2 pulses enables CK3, and completion of CK3 pulses enables CK4.

Id. at 5:18-20.

[33] *Id.* at 5:18-20.

capture clocks in both the '126 and '323 patents.[34] The term also is consistent with the applicants' generic use of the term "trigger" during prosecution of the '213 patent when discussing how the Nadeau-Dostie2 reference "triggered" its domains.[35]

Because the patentee relied on the claim requirement of "applying an ordered sequence of capture clock pulses" in "a sequential order" during prosecution to distinguish the prior art,[36] use of the trigger term is appropriate in the court's construction. At bottom, the foundation of the asserted patents is that the test in the second domain is triggered based on the completion of the test in the first domain – once the first domain is done, the second domain then is activated.[37]

2. A "Capture Clock" Should Not Be Limited to a "Test Clock"

The term "capture clock" appears multiple times in each asserted claim of each asserted

[34] *See* Docket No. 45-2, Ex. B at 23:20-24:2 ("capture clock pulses from two or more selected capture clocks placed in a sequential order such that all clock domains are never triggered simultaneously during a capture operation"); Docket No. 45-3, Ex. C at 22:53-56 (providing "capture clock pulses" in "a sequential order such that all clock domains are never triggered simultaneously during a capture operation").

[35] Ex. G to Cisco Opening Br. at ST000047

> '[A]ll' second domain clock pulses (see B1, B2, and B3 in FIG. 4) in Nadeau-Dostie2 must be aligned at the same positive edge so that they can be 'all' captured simultaneously, which leads to power consumption problems since all scan cells would be triggered simultaneously, every few cycles. In contrast, the present application, however, 'all' second domain clock pulses can be placed in a staggered order or in a sequential order.

See also id. at ST000050 (figure showing Nadeau-Dostie triggering all domain capture pulses simultaneously).

[36] Docket No. 45-7, Ex. G at ST000048. Although the prior art provided an alternative to triggering "clock suppression," Docket No. 47-5, Ex. E (Hetherington and Rajski Paper), that technique was identified during prosecution as problematic because the "shift clock pulses may also need precise timing alignment" and as "a result, it becomes quite difficult to perform at-speed self-test for designs containing clock domains operated at totally unrelated frequencies, e.g., 133 MHz and 60 Mhz." Docket No. 45-1, Ex. A at 3:15-18. To avoid this problem, the asserted patents explain that the invention "uses a daisy-chain clock triggering or token-ring clock enabling technique to generate and order capture clocks." Docket No. 45-1, Ex. A at 4:57-62, 5:34-40. This technique provides a "major benefit" enabling the use of asynchronous clock domains. *Id.* at 5:47-62. When daisy-chain or token-ring clocking is used, there is no need to align any capture clock or shift clock pulses, because each subsequent domain's capture clock pulse necessarily will be triggered after the occurrence of the previous domain's capture clock pulses.

[37] The language in the specification referring to programming does not constitute a third independent technique, but additional refinement to the daisy-chain or token-ring techniques described above – for example by altering the relative order in which the domains are applied.

patent. The parties generally agree that the term "capture clock" in the asserted patents means a "reconfigured system clock."[38] This construction is consistent with language from the asserted patents that the "reconfigured system clocks are called capture clocks."[39] The parties also agree that a single construction ought to control the same term's meaning across the family of patents.[40]

Despite this agreement, SynTest urges that the court substitute the term "capture clock" with the generic term "test clock." SynTest points to the patentees' use of "test clock" once during the prosecution history when referring to the capture clock. But this does not justify SynTest's proposed substitution.[41] When the patentees used the "test clock" term they were merely pointing out that the capture clock in these claims was being used to perform testing and that this particular capture clock was a special type of clock: a clock that provided both capture clock pulses and shift clock pulses, depending on the mode of operation:

> In many designs, a clock domain may be only controlled by one test clock. Thus, this test clock will contain clock pulses applied in scan mode (hence shift clock pulses) and clock pulses in normal mode (hence capture clock pulses).

While it is therefore true that the capture clock claimed in the asserted patents can be used during testing, it does not follow that every "test clock" is a capture clock as claimed in the asserted patents. Indeed, not every test clock is a "reconfigured system clock," which the parties have agreed and the patents confirm is the claimed "capture clock." And not every test clock is the special type that contains both capture clock pulses and shift clock pulses depending on the operational mode – as the patentees stressed the claimed "capture clock" was in this case.

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[38] *See* Docket No. 35, Ex. A at 1 ("capture clock(s)" in all asserted claims means "a reconfigured system clock").

[39] Docket No. 45-1, Ex. A at 9:20; *see also id.* at 1:47-50 (explaining that the patent's concept was to "take over control of all system clocks and reconfigure them as capture clocks").

[40] *See* Docket No. 46 at 10.

[41] *See id.* at 12.

The other justification for using the term "test clock" in this construction is the unremarkable observation that "external tests, like ATEs, are applicable to the present" invention[42] combined with a statement from the specification that, when "scan test is employed, the multiple-capture DFT system is usually resided in [sic] an ATE and, thus, all capture clocks are controlled externally."[43] There is no dispute, however, the reconfigured system clocks that are the "capture clocks" in the asserted patents can be generated internally or controlled externally. The patents explain that the system clocks can be generated inside of the circuit being tested or can be received from an external source at one of their input pins.[44] Whether generated internally or controlled externally, the capture clocks are reconfigured system clocks, and they are clocks that contain both shift clock pulses and capture clock pulses, depending on the operational mode.

In sum, construing the term capture clock to be a test clock is not warranted.

[42] Docket No. 46 at 12.

[43] Docket No. 45-1, Ex. A at 5:52-54.

[44] *Id*. at 1:34-35 ("Each system clock is either directly coming from a primary input (edge pin/connector) or generated internally.").

C. Dispute #3: "Applying an Ordered Sequence of Capture Clock Pulses to All Said Scan Cells Within Said N Clock Domains in Said Normal Mode During a Capture Operation, the Ordered Sequence of Capture Clock Pulses Comprising at Least Two Capture Clock Pulses From Two or More Selected Capture Clocks, for Controlling Two or More Clock Domains, in a Sequential Order"

CLAIM TERM/DISPUTE #3	
"applying an ordered sequence of capture clock pulses to all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture clock pulses comprising at least two capture clock pulses from two or more selected capture clocks, for controlling two or more clock domains, in a sequential order" The '213 patent (claims 1 and 29)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
"applying in a sequential order one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying another one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode for that next clock domain and continuing with this sequential order until the test is complete"	"triggering at least one clock domain's capture clock pulse in response to activity of another clock domain's capture clock pulse such that pulses from the capture clocks are received in a sequential order by all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture clock pulses comprising at least two capture clock pulses from two or more selected capture clocks, for controlling two or more clock domains"
CONSTRUCTION/RESOLUTION	
"applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode by triggering a capture clock pulse in the latter clock domain in response to a capture clock pulse in the former clock domain"	

Here, the parties dispute (1) whether "applying an ordered sequence" should be limited to "triggering" (2) whether the capture clock pulses must come from the capture clocks and (3) whether the pulses must be applied to each of N clock domains and (4) whether the phrase "without including shift clock pulses in the capture window" should be included.

In light of the central nature of the triggering concept to the asserted patents discussed above, triggering is included in the court's construction.

SynTest's proposed construction removes the requirement that "capture clock pulses" come "from two or more selected capture" clocks[45] and instead permits the capture clock pulses to come from anywhere. Its proposed construction also eliminates the requirement that the "ordered sequence of capture clock pulses" must be applied to "all scan cells within each of N clock domains of the integrated circuit or circuit assembly during a capture" operation[46] and refers to "continuing with this sequential order until the test is complete," an indefinite concept. Such a construction would provide an argument that a test is "complete," even where (1) capture clock pulses have not been applied to all scan cells within each of N clock domains (2) during a capture operation – features explicitly recited in the claim. These modifications are not warranted.

Cisco also urges the construction also inappropriately reintroduces claim limitations that the applicants deleted from the claims during prosecution in response to a claim rejection.[47] During prosecution of the '213 patent, the PTO specifically objected to the claim phase: "and does not contain any said shift clock pulse during a capture operation" as being not enabled. Patentees responded by deleting that phrase from the claims.[48] A construction that reads that limitation back into the claims is not warranted.[49]

But inspection of the prosecution history reveals such a narrow view of the claim language is not warranted. It is correct that, in response to the Examiner's Section 112 objection, the applicants deleted language from the claim and agreed with the Examiner's statement that only

[45] Docket No. 45-1, Ex. A at 23:32-33; 26:37-38 (requiring "at least two [said] capture clock pulses from two or more selected capture clocks").

[46] *See id.* at 23:28-29; 26:33-35.

[47] Twice the phrase "without including shift clock pulses in the capture window" – referring to pulses provided by a first and second selected capture clock – was deleted following a rejection.

[48] *See* Docket No. 45-7, Ex. G at ST000035, 44-45 (noting that Applicants deleted this language from the claims to obviate the Examiner's enablement rejections under § 112, first and second paragraph).

[49] *See, e.g., 3M Innovative Properties Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1372 (Fed. Cir. 2004) (refusing to import "sequential" claim limitation in the claim where patentee deleted the limitation in response to a rejection under 35 U.S.C. 112, second paragraph).

capture clock pulses can occur during the capture cycle, when the scan enable signal is inactive.[50] As pointed out to the Examiner during an interview with Dr. Wang and as demonstrated in the diagram Dr. Wang provided, however, the prior art recognizes a distinction between the capture cycle and the capture window or capture operation for purposes of fault testing.[51] Specifically, the prior art LOS methods for delay fault testing require that a last shift clock pulse launch the capture operation.[52] This distinction with the prior art is reflected in the specification.[53] Cisco failed to satisfy its burden of proof that SynTest "unequivocally disavowed a certain meaning to obtain his patent."[54]

[50] *See* Docket No. 45-7, Ex. G at ST000044-45.

[51] *See id.* at ST000050.

[52] *See id.* at ST000045-46.

[53] *See* Docket No. 45-1 at 3:8-11 (the approach discussed by Hetherington "rests on using multiple shift-followed-by-capture clocks each operating at its operating frequency, in a programmable capture window, to detect faults at-speed").

[54] *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed. Cir. 2003); *Am. Innotek, Inc. v. United States*, 113 Fed. Cl. 668, 677-79 (Fed. Cl. 2013) (review of statements to examiner and figures precluded a finding of disclaimer).

D. Dispute #4: "Applying an Ordered Sequence of Capture Clocks to All Said Scan Cells Within Said N Clock Domains, the Ordered Sequence of Capture Clocks Comprising at Least a Plurality of Capture Clock Pulses From Two or More Selected Capture Clocks Placed in a Sequential Order Such that All Clock Domains Are Never Triggered Simultaneously During a Capture Operation"

CLAIM TERM/DISPUTE #4	
"applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least a plurality of capture clock pulses from two or more selected capture clocks placed in a sequential order such that all clock domains are never triggered simultaneously during a capture operation" The '126 patent (claim 5) and the '323 patent (claim 1)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
"applying in a sequential order one or more capture clock pulses (without including shift clock pulses in the capture window) from a first selected test clock, which is derived from a first system clock, to the scan cells within a first one or more clock domains the first selected test clock controls, followed by applying another one or more capture clock pulses (without including shift clock pulses in the capture window) from a second selected test clock, which is derived from a second system clock, to the scan cells within a second one or more clock domains the second selected test clock controls, and continuing with this sequential order until the test is complete such that not all clock domains are ever activated simultaneously"	"triggering at least one clock domain's capture clock pulse in response to activity of another clock domain's capture clock pulse such that pulses from the capture clocks are received in a sequential order by all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least a plurality of capture clock pulses from two or more selected capture clocks and such that all clock domains are never triggered simultaneously during a capture operation"
CONSTRUCTION/RESOLUTION	
"applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode by triggering a capture clock pulse in the latter clock domain in response to a capture clock pulse in the former clock domain such that all clock domains are never triggered simultaneously during a capture operation"	

In addition to the disputes resolved in the two preceding constructions, dispute number four raises the additional issues of whether the construction should (1) delete "during a capture operation" from the claim – to prohibit simultaneous triggering even during the shift operation, (2) whether the term "activated" can be substituted for the term "triggered," (3) whether one

capture clock may control multiple clock domains and (4) whether the agreed construction of "capture clock" can be substituted with "test clock from which is derived a system clock."

This claim term is similar to the claim phrase reviewed above, except that it contains an additional requirement that "all clock domains are never triggered simultaneously during a capture operation." The court will not rehash its analysis above.

SynTests's construction of this term also deletes "during a capture operation" from the claim phrase "such that all clock domains are never triggered simultaneously during a capture operation." Although the claim specifically states the time period when all clock domains should not be simultaneously triggered – during a capture operation – the proposed construction removes that language from the claim so that the claims also prohibit simultaneously triggering clock domains during a shift operation. This construction that is inconsistent with the relevant specifications. For example, Figure 13 of the '323 patent illustrates that the first pulses in the shift cycle for all clocks are triggered simultaneously. The proposed construction transparently and retroactively sidesteps prior art: this is improper.

Without justification SynTest's proposed construction also substitutes the term "activated" for "triggered." Elsewhere in its argument, SynTest draws a distinction between "triggering" and other types of activation (e.g., enabling), but no accounting of the difference between the two is laid out in support of such a distinction. If "triggered" only referred to the very specific "daisy-chain" technique, it would be inappropriate to substitute the specific term "triggered" with a generic term "activated." Because the claim uses the term "triggered," the same term should be used in the construction.

United States District Court
For the Northern District of California

E. Dispute #5: Independent Claims 1 and 29 Do Not Require Delay Fault Testing to Be At Speed

CLAIM TERM/DISPUTE #5	
"when detecting or locating selected delay faults within a clock domain said selected capture clock controlling the clock domain contains at least two consecutive said capture clock pulses to launch the transition and capture the output response" The '213 patent (claims 1 and 29)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
"testing of delay faults is performed by applying two or more consecutive capture clock pulses to the clock domain with the first pulse initiating (launches) the transition, and the next one or more pulses that capture the output response at one or more scan cell(s)"	"when detecting or locating selected delay faults within a clock domain, said selected capture clock controlling the clock domain contains at least two consecutive said capture clock pulses generated at the domain's rated clock speed to launch the transition and capture the output response"
CONSTRUCTION/RESOLUTION	
"testing of delay faults is performed by applying two or more consecutive capture clock pulses to the clock domain with the first pulse initiating (launching) the transition at a targeted terminal and each subsequent pulse capturing the response at a scan cell"	

Cisco urges the delay fault testing must be done at speed, but SynTest counters this construction is inconsistent with dependent claim 15 that claims delay fault testing at speed. If at speed is read into the independent claims 1 and 29 and then dependent claim 15 is rendered a nullity under the doctrine of claim differentiation.[55]

The court agrees with SynTest. "The doctrine of claim differentiation is 'based on the common sense notion that different words or phrases used in separate claims are presumed to indicate that the claims have different meanings and scope.'"[56] "The doctrine is not a hard and fast

[55] *See* Docket No. 45-1, Ex. A

> 15. The method of claim 1, wherein said applying an ordered sequence of capture clock pulses further comprises selectively operating all said capture clock pulses controlling a selected clock domain at their rated clock speed, for detecting or locating delay faults within said selected clock

[56] *Starhome GmbH v. AT&T Mobility LLC*, Case No. 2012-1694, 2014 WL 685639, at *7 (Fed. Cir. Feb. 24, 2014) (quoting *Karlin Tech. Inc. v. Surgical Dynamics, Inc.*, 177 F.3d 968, 971-72 (Fed. Cir. 1999)).

rule, but instead "a rule of thumb that does not trump the clear import of the specification.'"[57] In this case, a common sense comparison of the independent and dependent claims shows that the additional requirement of default testing at speed should not be read into the claim.

F. Dispute #6: The Ordering of Claim Steps 1(a) Through 1(e) of Claim 1 of the '126 Patent

CLAIM TERM/DISPUTE #6	
The ordering of claim steps (a) through (e) in claim 1 of the '126 patent.	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
The order is not limiting and the elements can follow in any order.	The claimed steps must occur in the following order: 1(a), 1(b), 1(c), 1(d) and then 1(e).
CONSTRUCTION/RESOLUTION	
The claimed steps 1(a), 1(b) and 1(c) must precede steps 1(d) and 1(e).	

Claim 1 of the '126 patent provides for certain steps in a particular order:

(a) compiling the HDL code or netlist that represents said integrated circuit or circuit assembly in physical form into a design database;

(b) performing test rule check for checking whether said design database contains any multiple-capture rule violations in said scan-test or said self-test mode;

(c) performing test rule repair until all said multiple-capture rule violations have been fixed;

(d) performing multiple-capture test synthesis for generating a testable HDL code or netlist; and

(e) generating HDL test benches and automatic test equipment (ATE) test programs for verifying the correctness of said testable HDL netlist in said scan-test or said self-test mode.[58]

The parties dispute whether the method claim elements listed above must be performed in order.[59] SynTest urges that for the order of a method claim to be binding it must be "unequivocally

[57] *Id.* (quoting *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1332 (Fed. Cir. 2009)); *see also Netcraft Corp. v. eBay, Inc.*, 549 F.3d 1394, 1400 n.1 (Fed. Cir. 2008) ("While claim differentiation may be helpful in some cases, it is just one of many tools used by courts in the analysis of claim terms.").

[58] *See* Docket No. 45-2, Ex. B at 22:39-64.

[59] Although "a method claim necessarily recites the steps of the method in a particular order, as a general rule the claim is not limited to performance of the steps in the order recited, unless the claim explicitly or implicitly requires a specific order." *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1345 (Fed. Cir. 2008) (citing *Interactive Gift Express, Inc. v. Compuserve Inc.*, 256

dictated;"[60] but *Baldwin Graphics* does not support such a per se requirement. The *Baldwin* court's holding was milder: the claim need only "implicitly or explicitly" require a specific order in light of the specification.[61] Here, all of the multiple-capture rule violations must be identified before steps (d) and (e) may be completed. It is insufficient for any violation to be missed, because the resulting netlist then may not detect the faults in design. The court holds – and the parties agreed at oral argument – that not all violations must be identified before each may be fixed – step B need not be completed, in its entirety, before Step C is performed.

G. Dispute #7: The Meaning of Checking Whether Said Design Database Contains Any Multiple Capture Violations

CLAIM TERM/DISPUTE #7	
The meaning of checking whether said design database contains any multiple capture violations The '126 patent (claim 1)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
"verifying whether the design complies with scan and BIST-specific design rules"	"identifying each multiple capture rule violation that exists in the design database"
CONSTRUCTION/RESOLUTION	
verifying whether the design complies with scan and BIST-specific design rules.	

In the design of an ASIC, the goal is to fix all rule violations. The parties dispute whether the claim requires all rule violations to be identified before all identified rule violations can be fixed. The dispute with respect to whether such an ordering is required turns on whether "'any' multiple-capture rule violation as used in the Claim step 1(b) refers to 'all' multiple capture

F.3d 1323, 1342-43 (Fed. Cir. 2001). Despite that backdrop, the "specification or prosecution history" may "require a narrower, order-specific construction of a method claim in some cases." *Id.* (citing *Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1342-43 (Fed. Cir. 2001).

[60] *See* Docket No. 50 at 22 (citing *Baldwin Graphic*, 512 F.3d at 1345).

[61] *See supra* note 59.

violations."[62] If after a review, no multiple-capture rule violations are found, the next step of fixing all rule violations is completed by doing nothing. Similarly, Cisco's reference to the use of the word "any" in the specification as it relates to clock skews is simply unavailing. The term "any" is used repeatedly in the claim language itself, without signifying all is meant. For example, the preamble states that what is claimed is an "apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains."[63] Any cannot mean all in this context. Similarly, one dependent claim includes the phrase "applying said capture clock pulses concurrently to two or more selected clock domains which do not interact with each other or do not have any logic block crossing."[64] Any could not mean all in this context, either.

The parties agree that multiple-capture refers to a method for delay testing.[65] Cisco does not contend that there is anything indefinite about the term "rule violations" as it relates to delay fault testing of an ASIC in design. One "of ordinary skill in the relevant art could not discern" that multiple-capture rules violations refer to delay testing violations that would apply to the multiple-capture methods of delay fault testing.[66]

[62] Docket No. 51 at 24.

[63] Docket No. 45-3 at 22:39-31.

[64] *See id.* at 23:28-30.

[65] Docket No. 51 at 25:7-10.

[66] *Haliburton Entergy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1249-1250 (Fed. Cir. 2008).

H. Dispute #8: "Each Shift Clock Pulse Comprising a Clock Pulse Applied in Scan Mode"

CLAIM TERM/DISPUTE #8	
"each shift clock pulse comprising a clock pulse applied in scan mode" The '213 patent (claims 1, 29) and the '126 patent (claim 1)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
"each waveform from a clock which generates a shift clock pulse at a frequency that need not be at the same speed as the normal operating frequency of that domain's system clock"	"each shift clock pulse comprising a pulse of the capture clock applied while a scan enable signal for the clock domain is asserted"
CONSTRUCTION/RESOLUTION	
"each shift clock pulse comprising a pulse of the capture clock at a frequency that need not be the same as the normal operating frequency of the domain's system clock"	

The parties agree that "each shift clock pulse comprising a clock pulse applied in scan mode" can be construed as a pulse of a test clock when scan enable is active. Cisco attempts to limit the clock that can generate this pulse to a reconfigured system clock, the same clock generating the capture clock pulses with both the shift clock pulses and the capture clock pulses being generated at the same frequency. This construction ignores the specification, which identifies the reach of the invention to embrace both self-test and scan-test.[67] Additionally, the specification recognizes that separate clocks can be responsible for shift clock pulses and capture clock pulses.[68] As Cisco acknowledges, while adequate delay fault testing requires capture clock pulses be at-speed[69] "the shifting frequency is irrelevant to at-speed testing."[70] This is because "testing of delay faults at-speed [with this invention] is now performed by applying two

[67] *See* Docket No. 45-1, Ex. A at 4:39-42 ("This invention applies to any self-test or scan-test method that requires multiple capture clock pulses (without including shift clock pulses) in the capture cycle.").

[68] *See id.* at 5:28-32.

[69] *See* Docket No. 44 at 18:2-20.

[70] *See id.* at 19:6-9 (quoting Docket No. 45-1, Ex. A at 4:19-22).

consecutive capture clock pulses (double captures) rather than using the shift followed- by-capture clock pulses."[71]

I. Dispute #9: "Each Capture Clock Pulse Comprising a Clock Pulse Applied in Normal Mode"

CLAIM TERM/DISPUTE #9	
"each capture clock pulse comprising a clock pulse applied in normal mode" The '213 patent (claims 1, 29) and the '126 patent (claim 1)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
"each waveform from a clock which generates capture clock pulses that need not be at the same speed as the clock when generating shift clock pulses"	"each capture clock pulse comprising a pulse of the capture clock applied while a scan enable signal for the clock domain is not asserted"
CONSTRUCTION/RESOLUTION	
"each capture clock pulse comprising a pulse of the capture clock at a frequency that need not be the same as the clock when generating shift clock pulses"	

The discussion to dispute number eight applies with equal force to dispute number nine.

[71] *See id.* at 4:49-52.

J. What Means-Plus-Function Structures are Disclosed in the Specification of the '323 Patent

CLAIM TERM/DISPUTE #10	
What structures are disclosed by the specification with respect to "means for generating and shifting-in N test stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during a shift-in operation" The '323 patent (claim 1)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
Means: Generating test stimuli **Structure:** If self-test – PRPG is responsible for generating N Test stimuli. Use of a phase shifter is optional. If scan-test – ATPG is responsible for generating N Test stimuli **Means:** for shifting-in test stimuli **Structure:** If self-test – the DFT system controls the operation and can utilize the system clock or any other clock. If scan-test – the ATE	**Means:** Generating test stimuli **Structure:** PRPG combined with a phase shifter **Means:** for shifting in test stimuli **Structure:** The reconfigured system clock
CONSTRUCTION/RESOLUTION	
Function: Generating N test stimuli. **Structure:** If self-test – the PRPG with or without a phase shifter. If scan-test – the ATPG. **Function:** Shifting-in N test stimuli. **Structure:** If self-test – the DFT system. If scan-test – the ATE.	

Because the parties agree on the function, the only issue before the court is the corresponding structure. The parties agree that there are two elements to the structure: (1) generating N test stimuli and (2) shifting in N test stimuli to all said scan cells. With respect to the first structure, Cisco contends that "the specification unambiguously explains that PRPGs combined with phase shifters are used to generate test stimuli."[72] Cisco ignores that the phase shifters are identified as "optional" by the patent.[73] Moreover, by citing only to the PRPG, Cisco again attempts to limit the invention to self-test. A PRPG is not a requirement for scan-test.

[72] Docket No. 44 at 21:15-16.

[73] Docket No. 45-3 at 22:5-7 ("Each PRPG-MISR pair is composed of a PRPG, an optional phase shifter, an optional space compactor, a MISR, and a comparator.").

Cisco identifies the "capture clock" as the structure for the second element citing that "[d]uring each shift cycle" a "series of pulses" are "applied through capture clocks" to shift stimuli to all scan cells within all clock" domains.[74] Cisco again cites to the capture clock in an effort to read out scan-test, which is inappropriate for all the reasons discussed above.

By contrast, and to address the fact that the invention covers both scan-test and self-test, SynTest identified the DFT system as the structure for both the generation of test stimuli and the shifting in of data. The specification explicitly supports this structure as performing both functions in both scan-test and self-test.[75] SynTest argues that the shifting operation is different from the capture operation and the clocks therefore need not be at the same speeds and can originate from different clocks. Cisco's construction improperly requires a scan-enabled system, but the claim language does not require this limitation.

The court agrees that scan design is not completely dependent upon the use of a scan-enabled signal. While the use of a scan-enabled signal may be the most common way to shift data in and out of a scan chain during test, the specification makes clear that the "multiple-capture DFT system of the present invention further comprises any method or apparatus for performing the shift operation at any selected clock speed within each clock" domain.[76] The specification also recognizes that separate clocks can generate shift clock pulses and capture clock pulses.[77] Cisco's additional limitations are unwarranted.

[74] *See* Docket No. 44 at 19:16-18 (quoting Docket No. 45-1, Ex. A at 10:47-50).

[75] *See* Docket No. 45-3, Ex. C at 9:16-20 ("During the shift operation, the multiple-capture DFT system first generates and shifts pseudorandom or predetermined stimuli through all scan cells SC in all scan chains SCN . . . ."); 5:46-50 ("When self-test is employed, the multiple-capture DFT system is usually placed inside the integrated circuit . . . . When scantest is employed, the multiple-capture DFT system is usually resided in an ATE.").

[76] *See* Docket No. 45-1, Ex. A at 4:31-33.

[77] *See id.* at 5:28-32.

IT IS SO ORDERED.

Dated: June 9, 2014

PAUL S. GREWAL
United States Magistrate Judge

US007007213B2

(12) United States Patent
Wang et al.

(10) **Patent No.: US 7,007,213 B2**
(45) **Date of Patent: Feb. 28, 2006**

(54) **MULTIPLE-CAPTURE DFT SYSTEM FOR DETECTING OR LOCATING CROSSING CLOCK-DOMAIN FAULTS DURING SELF-TEST OR SCAN-TEST**

(75) Inventors: **Laung-Terng (L.-T.) Wang**, Sunnyvale, CA (US); **Po-Ching Hsu**, Hsinchu (TW); **Shih-Chia Kao**, Taipei (TW); **Meng-Chyi Lin**, Taoyuan (TW); **Hsin-Po Wang**, Hsinchu (TW); **Hao-Jan Chao**, Taoyuan (TW); **Xiaoqing Wen**, Sunnyvale, CA (US)

(73) Assignee: **Syntest Technologies, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 619 days.

(21) Appl. No.: **10/067,372**

(22) Filed: **Feb. 7, 2002**

(65) **Prior Publication Data**

US 2002/0120896 A1 Aug. 29, 2002

Related U.S. Application Data

(60) Provisional application No. 60/268,601, filed on Feb. 15, 2001.

(51) **Int. Cl.**
G01R 31/28 (2006.01)

(52) **U.S. Cl.** **714/729**; 714/731

(58) **Field of Classification Search** 714/729, 714/731

See application file for complete search history.

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U.S. Appl. No. 2003/0097614 A1 Rajski et al. filed May 22, 2003.

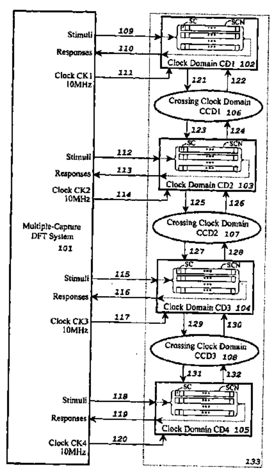
* cited by examiner

Primary Examiner—Joseph D. Torres
(74) *Attorney, Agent, or Firm*—Jim Zegeer

(57) **ABSTRACT**

A method and apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in self-test or scan-test mode, where N>1 and each domain has a plurality of scan cells. The method and apparatus allows generating and loading N pseudorandom or predetermined stimuli to all the scan cells within the N clock domains in the integrated circuit or circuit assembly during the shift operation, applying an ordered sequence of capture clocks to all the scan cells within the N clock domains during the capture operation, compacting or comparing N output responses of all the scan cells for analysis during the compact/compare operation, and repeating the above process until a predetermined limiting criteria is reached. A computer-aided design (CAD) system is further developed to realize the method and synthesize the apparatus.

30 Claims, 25 Drawing Sheets



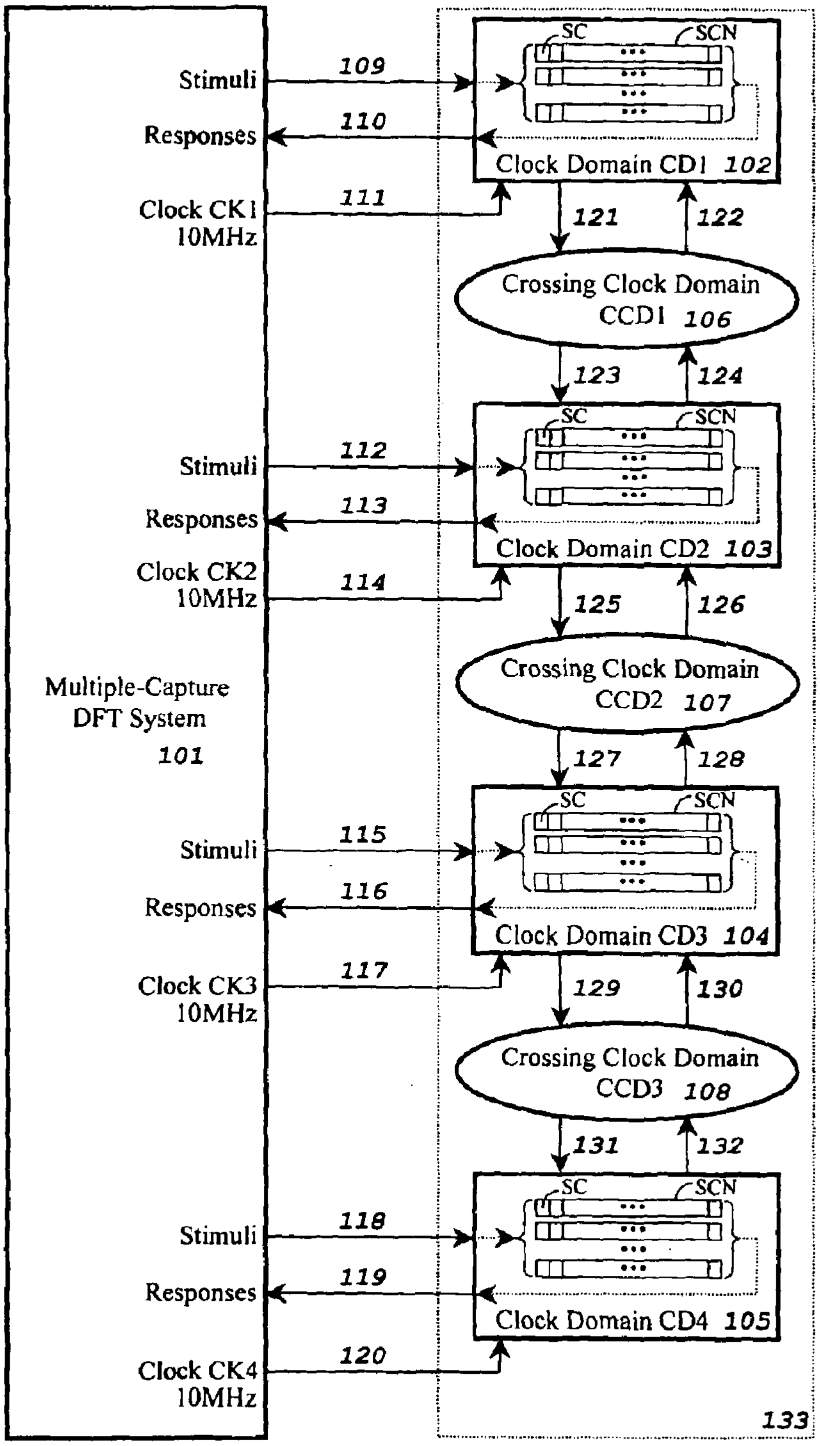

Stimuli
Responses
Clock CK1
10MHz
109
110
111
SC
SCN
Clock Domain CD1 102
121
122
Crossing Clock Domain
CCD1 106
123
124
Stimuli
Responses
Clock CK2
10MHz
112
113
114
Clock Domain CD2 103
125
126
Crossing Clock Domain
CCD2 107
Multiple-Capture
DFT System
101
127
128
Stimuli
Responses
Clock CK3
10MHz
115
116
117
Clock Domain CD3 104
129
130
Crossing Clock Domain
CCD3 108
131
132
Stimuli
Responses
Clock CK4
10MHz
118
119
120
Clock Domain CD4 105
133

FIG. 1

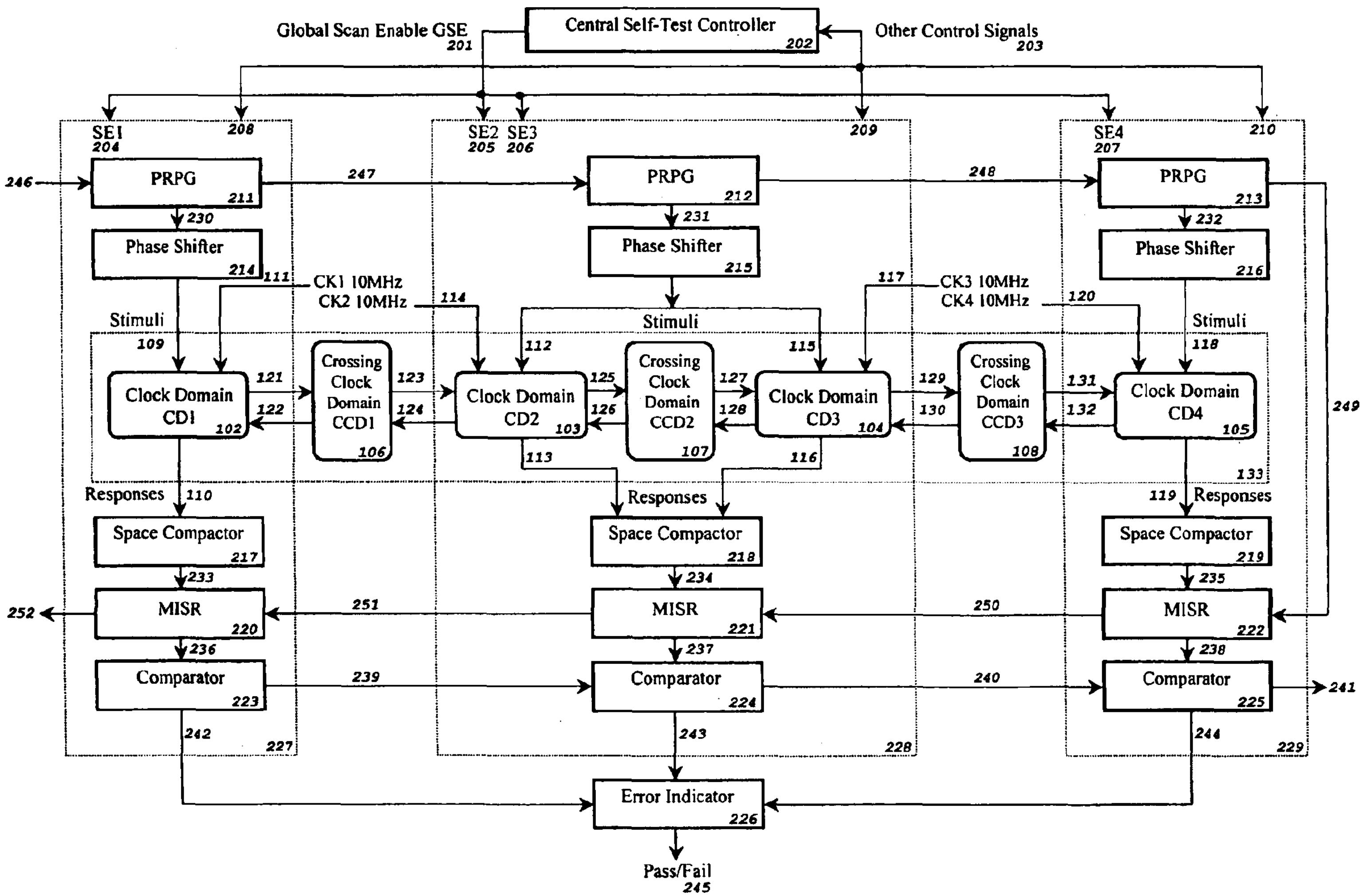

Central Self-Test Controller 202
Global Scan Enable GSE 201
Other Control Signals 203
SE1 204
208
SE2 205
SE3 206
209
SE4 207
210
246
PRPG 211
247
PRPG 212
248
PRPG 213
230
231
232
Phase Shifter 214
Phase Shifter 215
Phase Shifter 216
111
CK1 10MHz
CK2 10MHz
114
117
CK3 10MHz
CK4 10MHz
120
Stimuli 109
Stimuli
Stimuli 118
112
115
Clock Domain CD1 102
121
122
Crossing Clock Domain CCD1 106
123
124
Clock Domain CD2 103
125
126
Crossing Clock Domain CCD2 107
127
128
Clock Domain CD3 104
129
130
Crossing Clock Domain CCD3 108
131
132
Clock Domain CD4 105
249
113
116
133
Responses 110
Responses
119 Responses
Space Compactor 217
Space Compactor 218
Space Compactor 219
233
234
235
252
MISR 220
251
MISR 221
250
MISR 222
236
237
238
Comparator 223
239
Comparator 224
240
Comparator 225
241
242
227
243
228
244
229
Error Indicator 226
Pass/Fail 245

FIG. 2

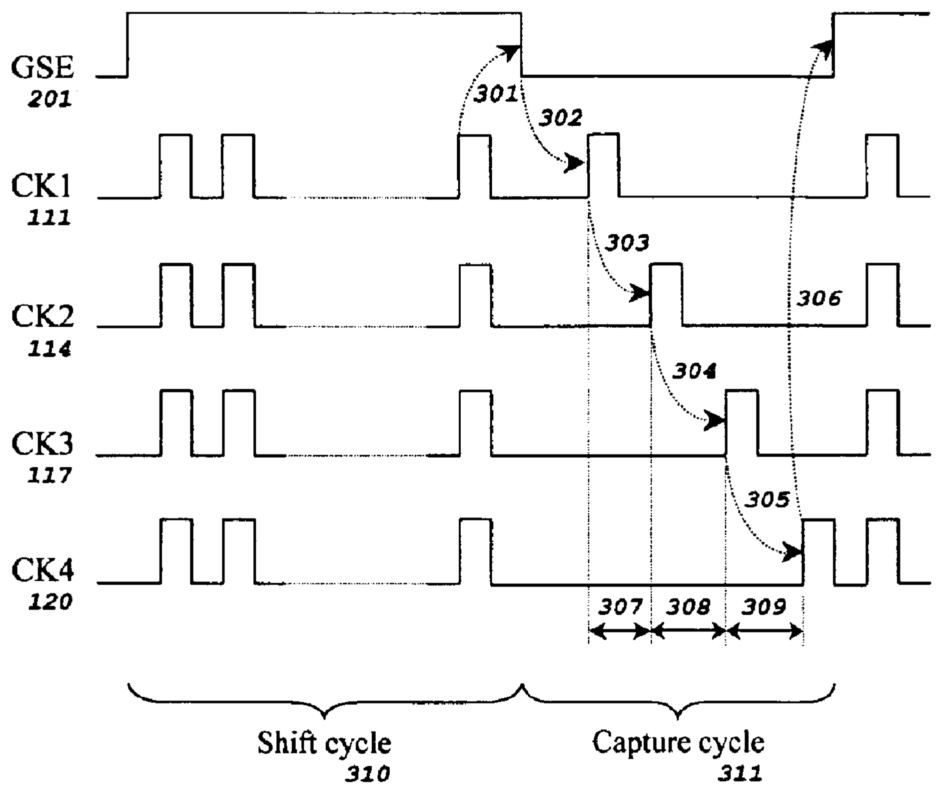

GSE
201
CK1
111
CK2
114
CK3
117
CK4
120
301
302
303
304
305
306
307
308
309
Shift cycle
310
Capture cycle
311

FIG. 3

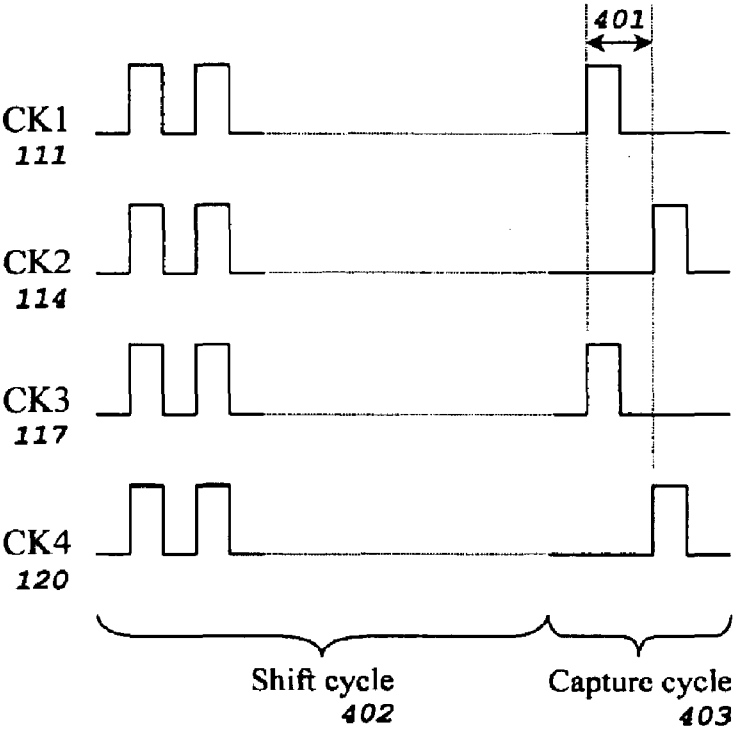

401
CK1
111
CK2
114
CK3
117
CK4
120
Shift cycle
402
Capture cycle
403

FIG. 4

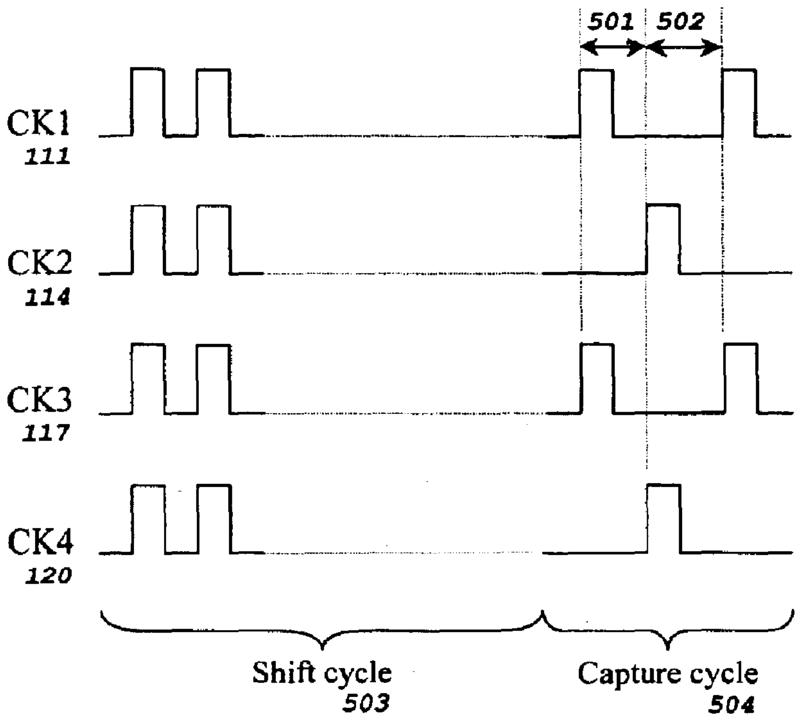

501
502
CK1
111
CK2
114
CK3
117
CK4
120
Shift cycle
503
Capture cycle
504

FIG. 5

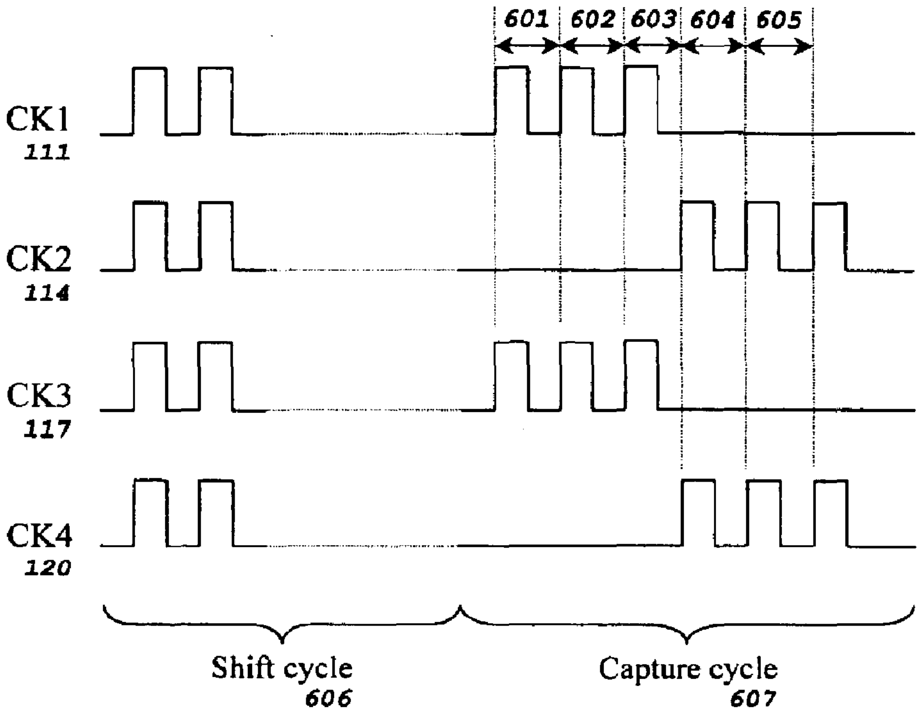

601
602
603
604
605
CK1
111
CK2
114
CK3
117
CK4
120
Shift cycle
606
Capture cycle
607

FIG. 6

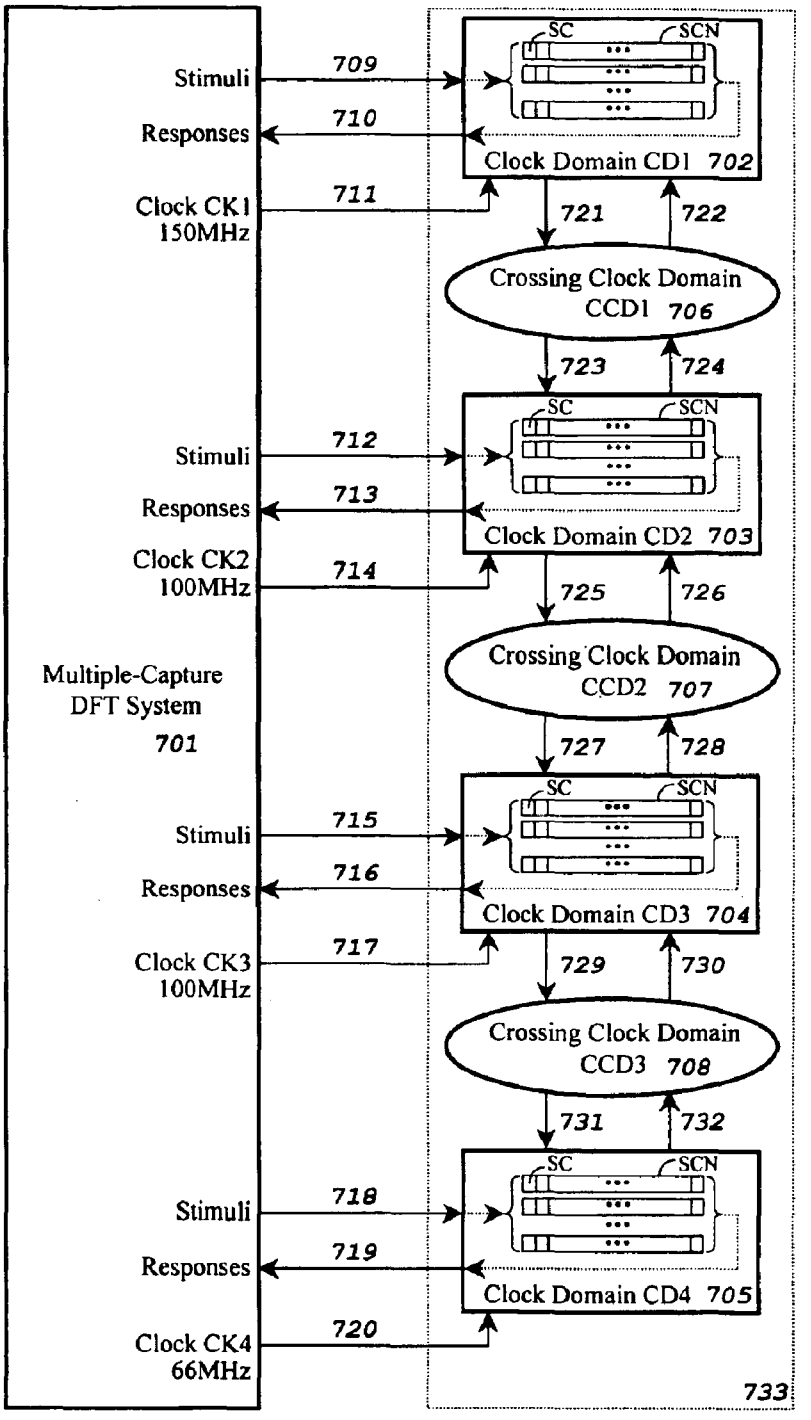

Stimuli
709
Responses
710
Clock CK1
150MHz
711
SC
SCN
Clock Domain CD1 702
721
722
Crossing Clock Domain
CCD1 706
723
724
Stimuli
712
Responses
713
Clock CK2
100MHz
714
Clock Domain CD2 703
725
726
Crossing Clock Domain
CCD2 707
727
728
Multiple-Capture
DFT System
701
Stimuli
715
Responses
716
Clock CK3
100MHz
717
Clock Domain CD3 704
729
730
Crossing Clock Domain
CCD3 708
731
732
Stimuli
718
Responses
719
Clock CK4
66MHz
720
Clock Domain CD4 705
733

FIG. 7

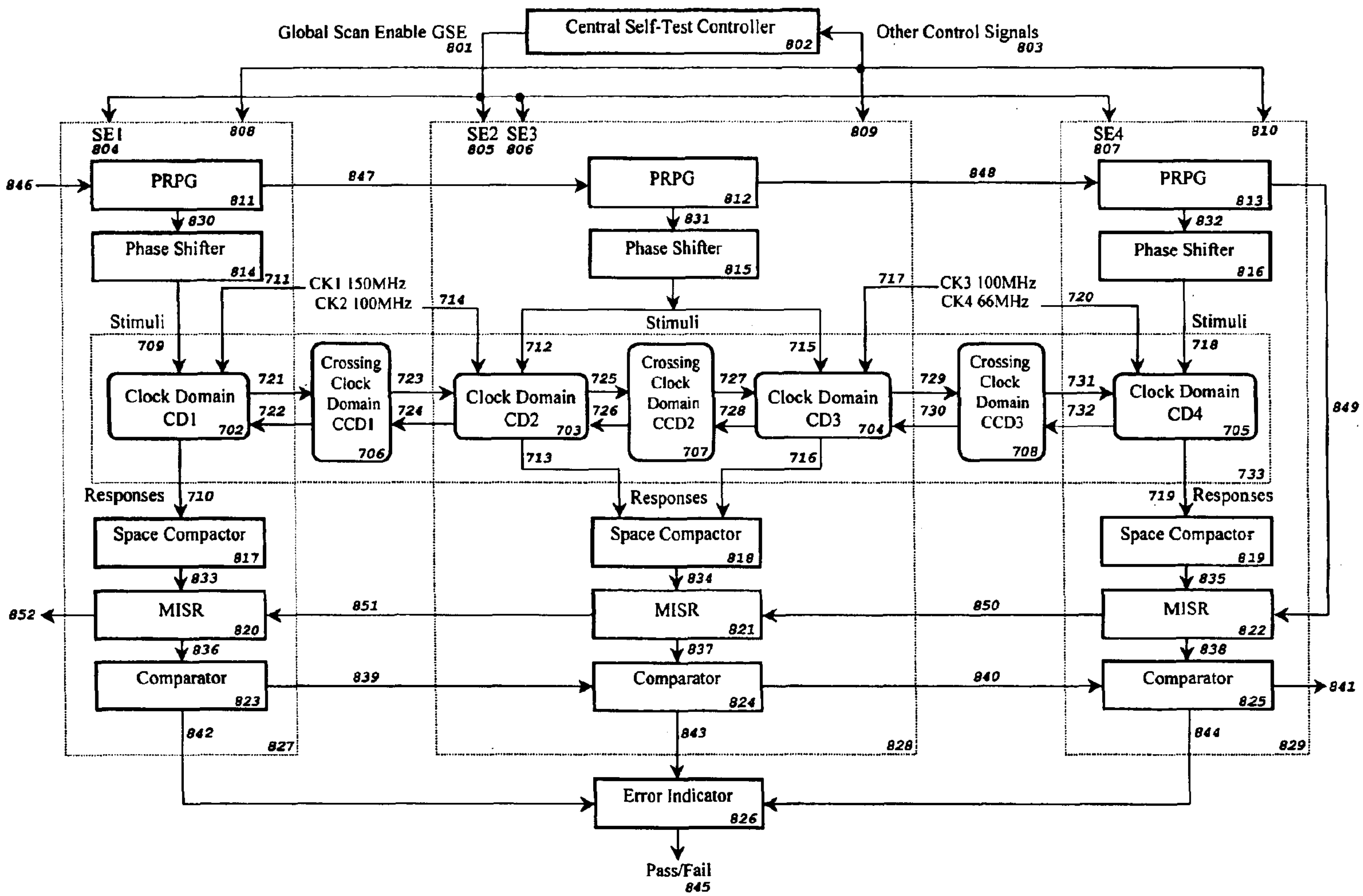

Central Self-Test Controller
802
Global Scan Enable GSE
801
Other Control Signals
803
SE1
804
808
SE2
805
SE3
806
809
SE4
807
810
846
PRPG
811
847
PRPG
812
848
PRPG
813
830
831
832
Phase Shifter
814
Phase Shifter
815
Phase Shifter
816
711
CK1 150MHz
CK2 100MHz
714
717
CK3 100MHz
CK4 66MHz
720
Stimuli
709
Stimuli
712
715
Stimuli
718
Clock Domain CD1
702
721
722
Crossing Clock Domain CCD1
706
723
724
Clock Domain CD2
703
725
726
Crossing Clock Domain CCD2
707
727
728
Clock Domain CD3
704
729
730
Crossing Clock Domain CCD3
708
731
732
Clock Domain CD4
705
849
713
716
733
Responses
710
Responses
719
Responses
Space Compactor
817
Space Compactor
818
Space Compactor
819
833
834
835
852
MISR
820
851
MISR
821
850
MISR
822
836
837
838
Comparator
823
839
Comparator
824
840
Comparator
825
841
842
827
843
828
844
829
Error Indicator
826
Pass/Fail
845

FIG. 8

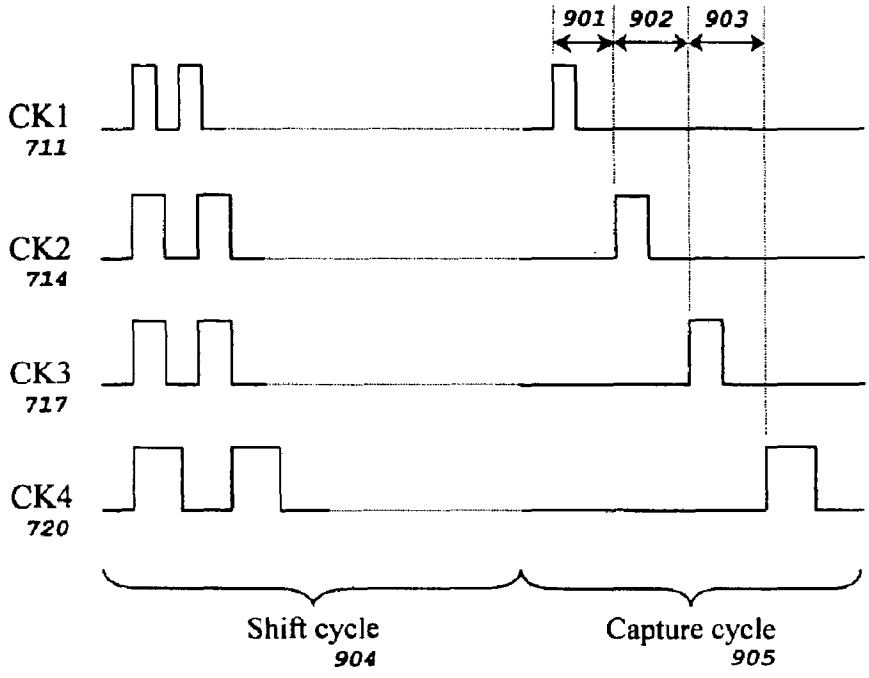

901
902
903
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
904
Capture cycle
905

FIG. 9

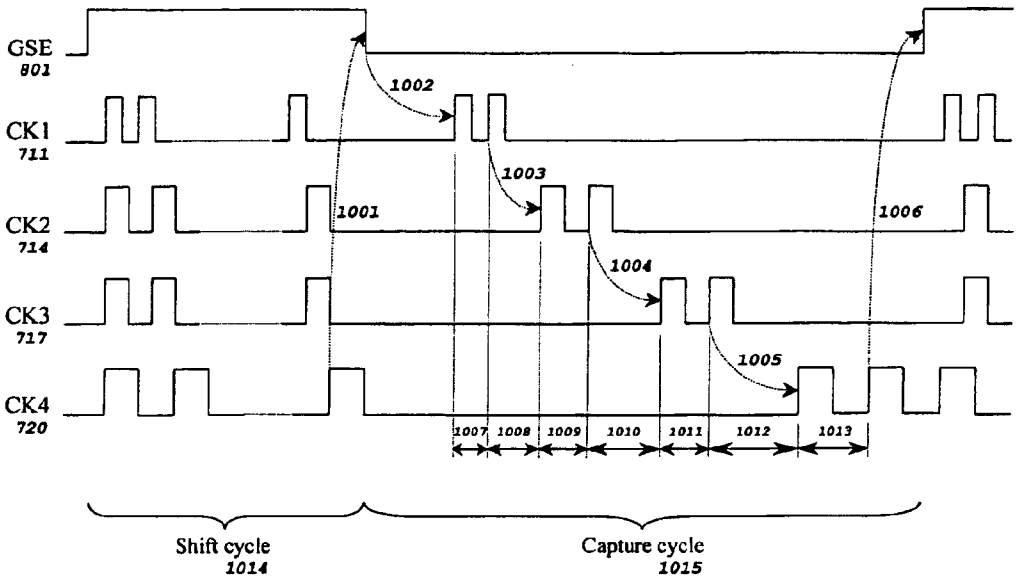

GSE
801
CK1
711
CK2
714
CK3
717
CK4
720
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
Shift cycle
1014
Capture cycle
1015

FIG. 10

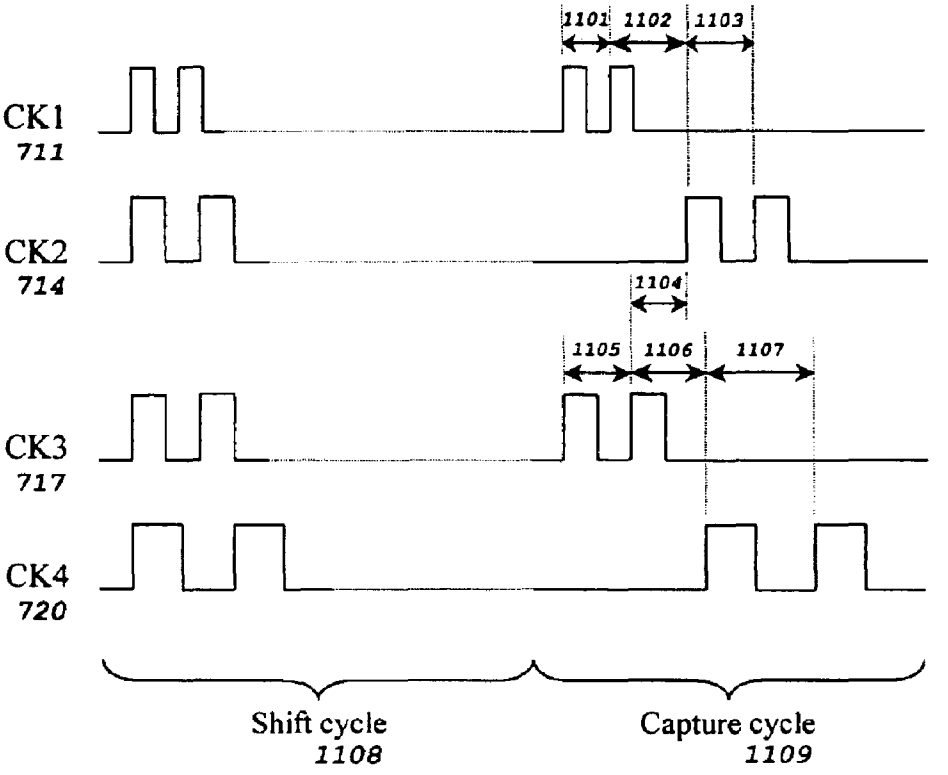

1101
1102
1103
CK1
711
CK2
714
1104
1105
1106
1107
CK3
717
CK4
720
Shift cycle
1108
Capture cycle
1109

FIG. 11

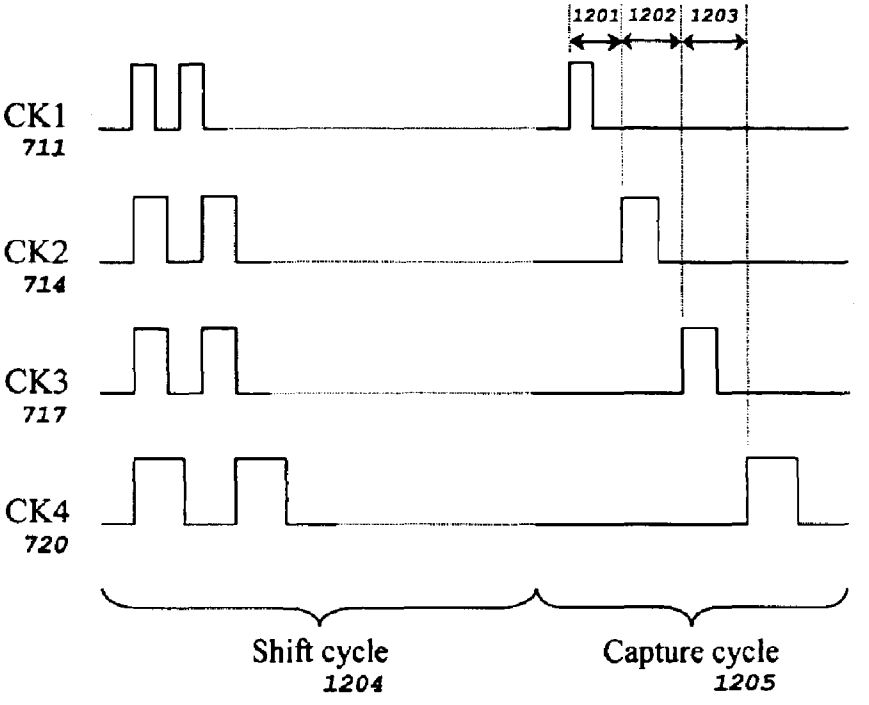

1201
1202
1203
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1204
Capture cycle
1205

FIG. 12

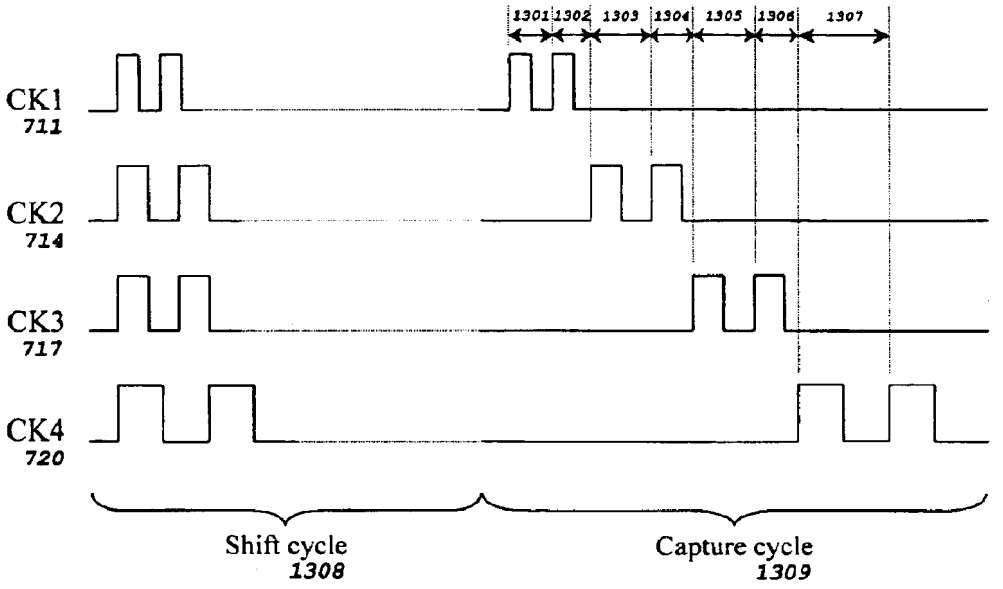

1301
1302
1303
1304
1305
1306
1307
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1308
Capture cycle
1309

FIG. 13

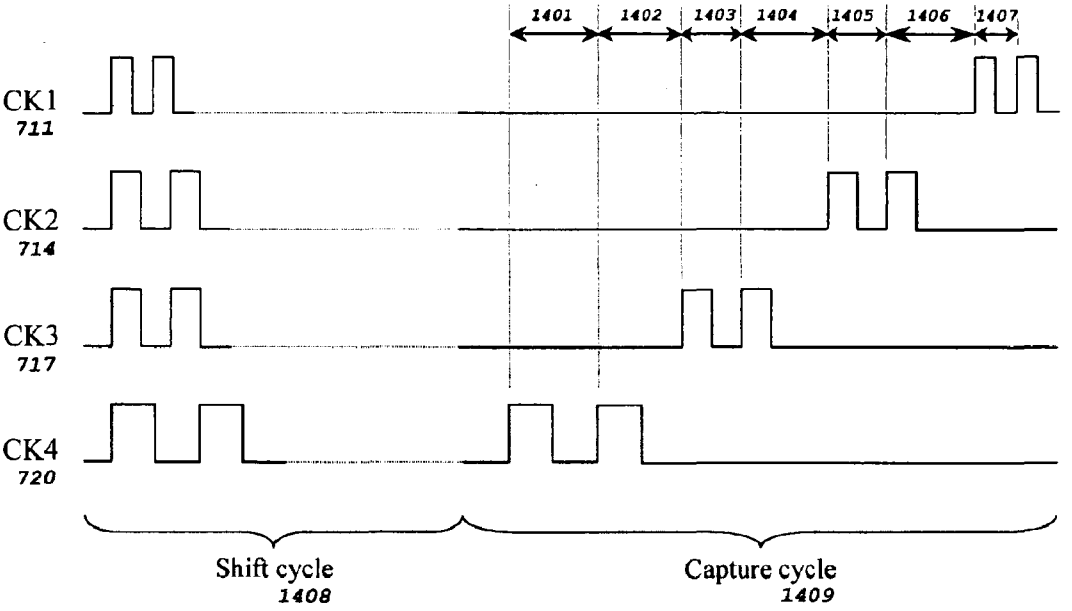

1401
1402
1403
1404
1405
1406
1407
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1408
Capture cycle
1409

FIG. 14

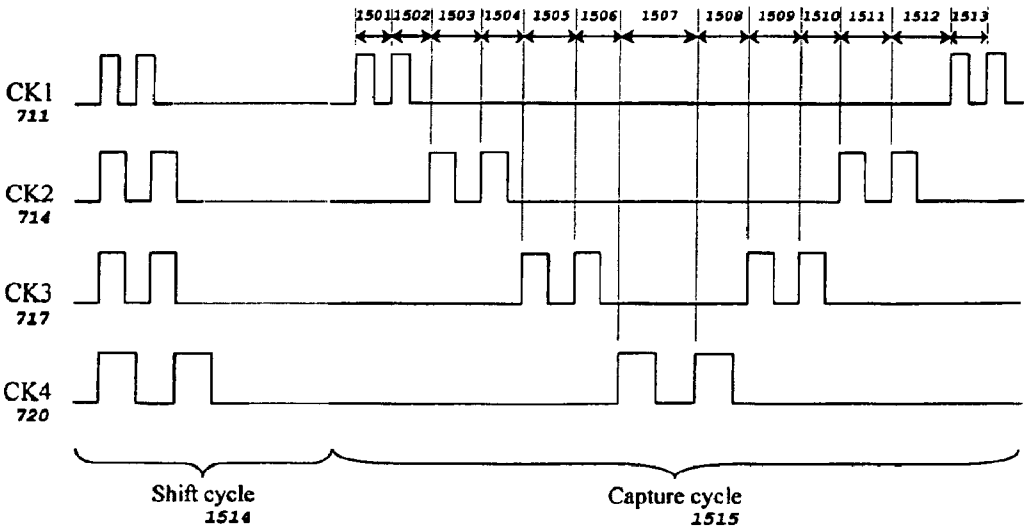

1501 1502 1503 1504 1505 1506 1507 1508 1509 1510 1511 1512 1513
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1514
Capture cycle
1515

FIG. 15

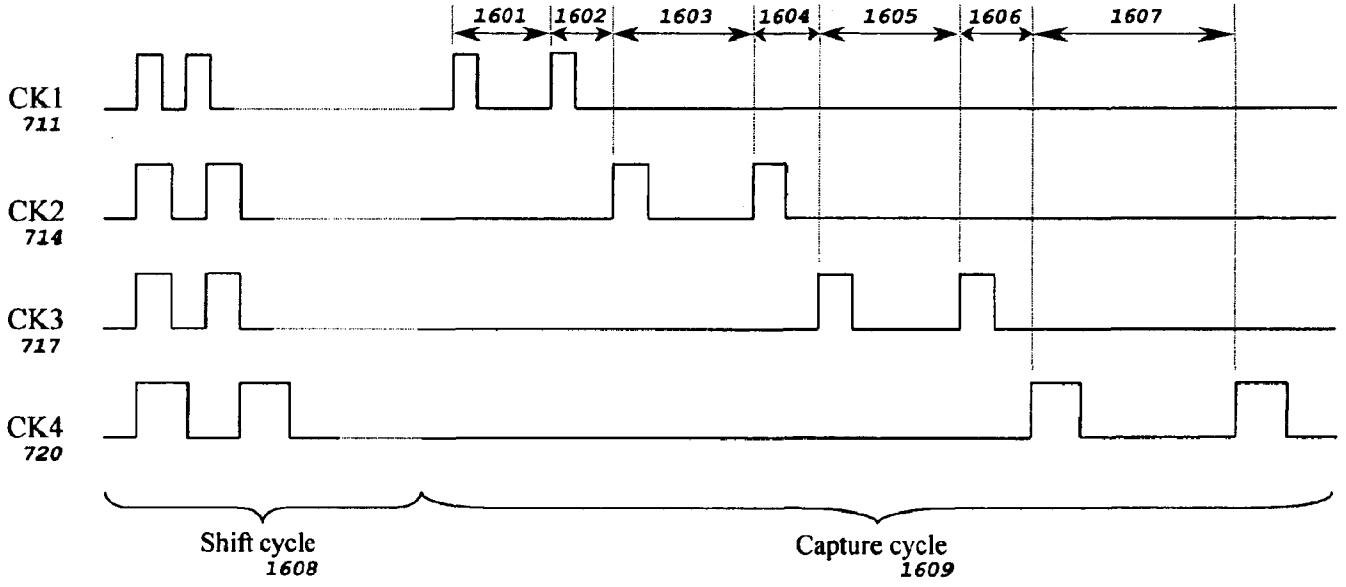

1601
1602
1603
1604
1605
1606
1607
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1608
Capture cycle
1609

FIG. 16

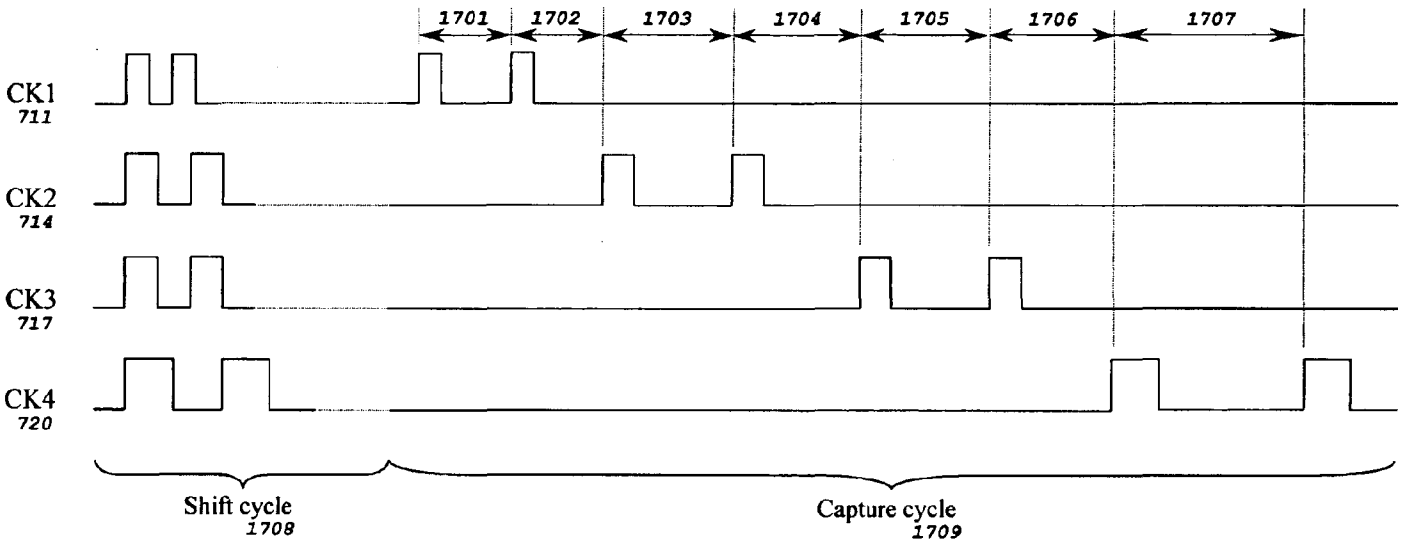

1701
1702
1703
1704
1705
1706
1707
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1708
Capture cycle
1709

FIG. 17

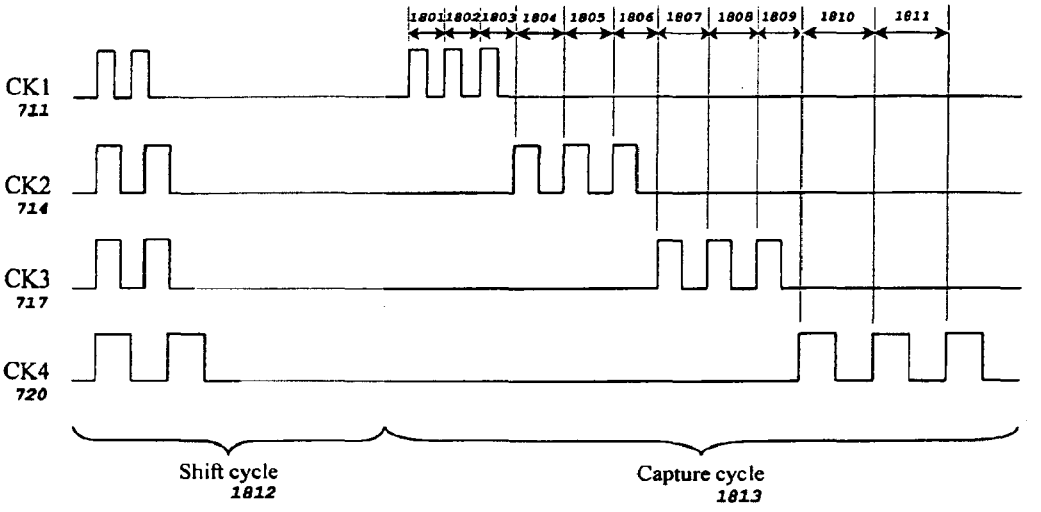

1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1812
Capture cycle
1813

FIG. 18

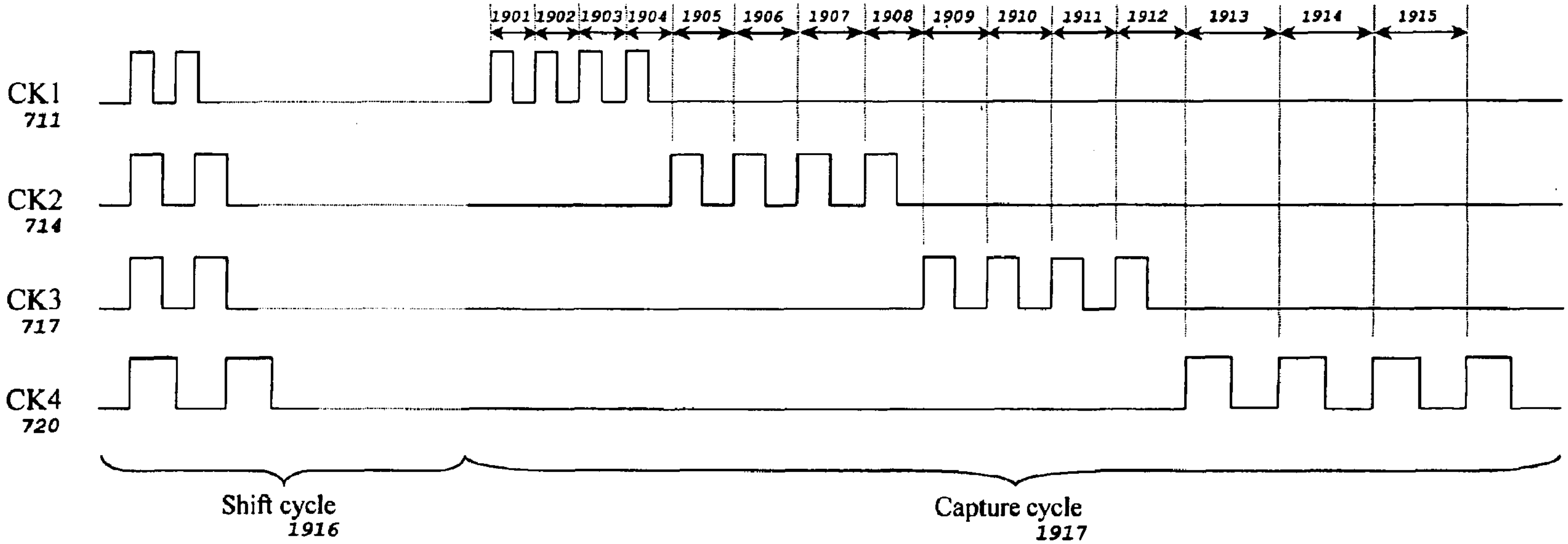

1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1916
Capture cycle
1917

FIG. 19

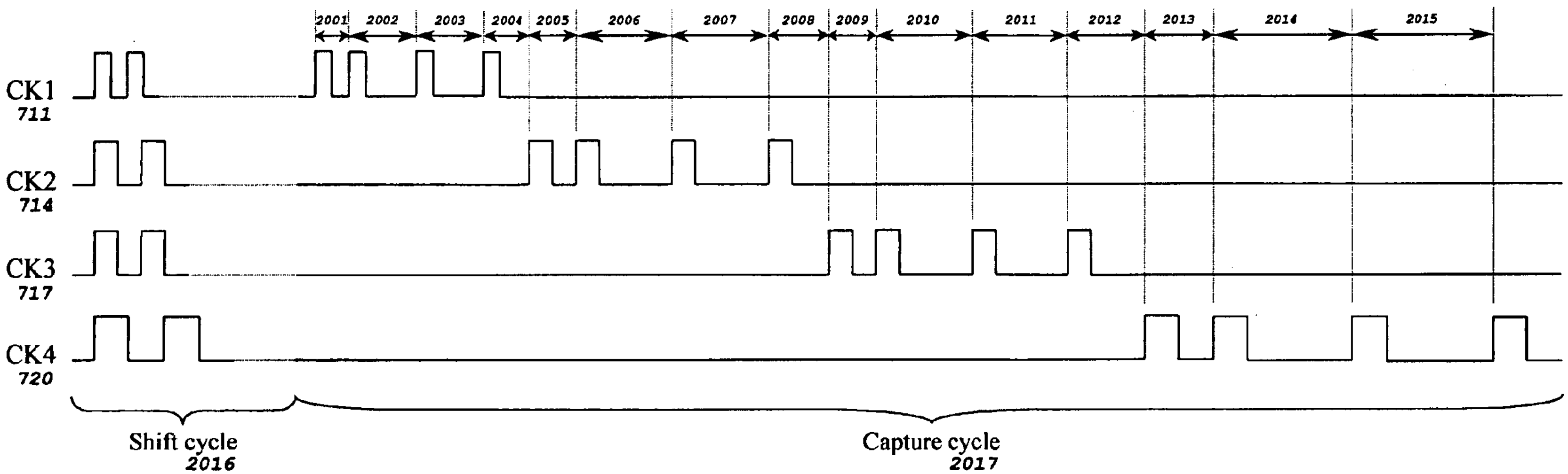

2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
2016
Capture cycle
2017

FIG. 20

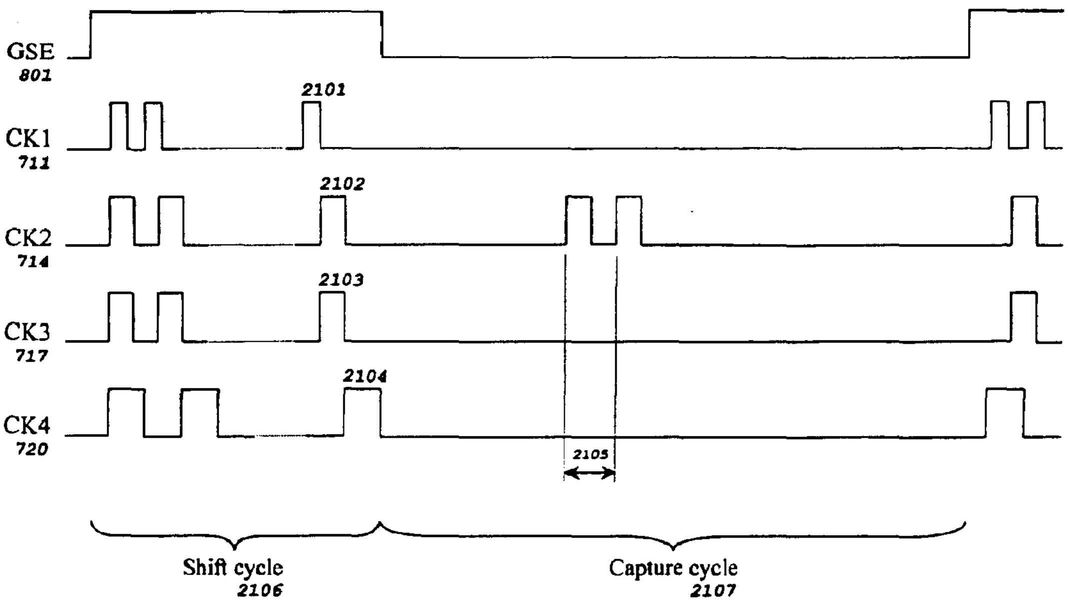

GSE
801
CK1
711
2101
CK2
714
2102
CK3
717
2103
CK4
720
2104
2105
Shift cycle
2106
Capture cycle
2107

FIG. 21

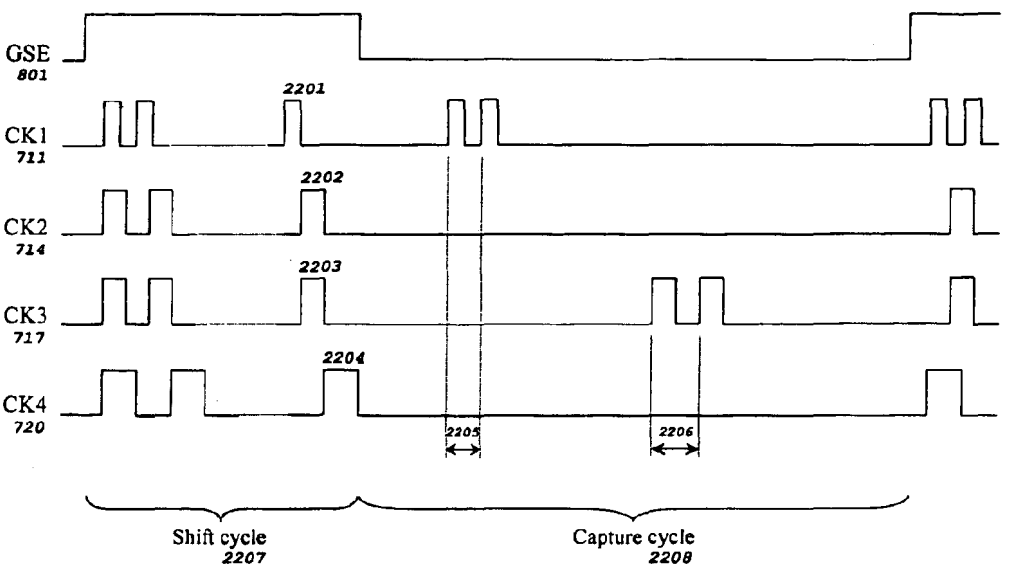

GSE
801
2201
CK1
711
2202
CK2
714
2203
CK3
717
2204
CK4
720
2205
2206
Shift cycle
2207
Capture cycle
2208

FIG. 22

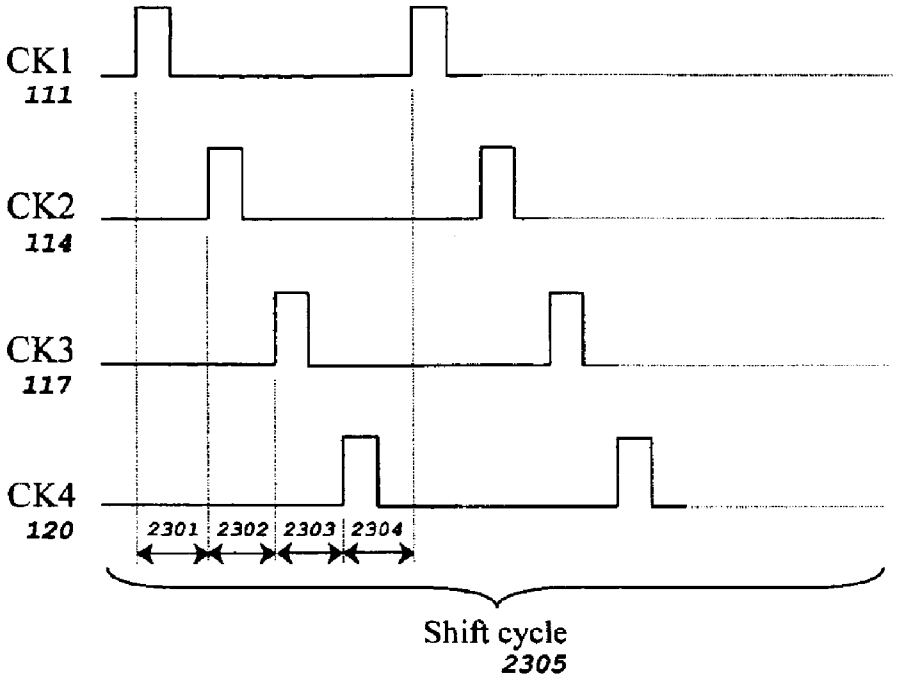

CK1
111
CK2
114
CK3
117
CK4
120
2301
2302
2303
2304
Shift cycle
2305

FIG. 23

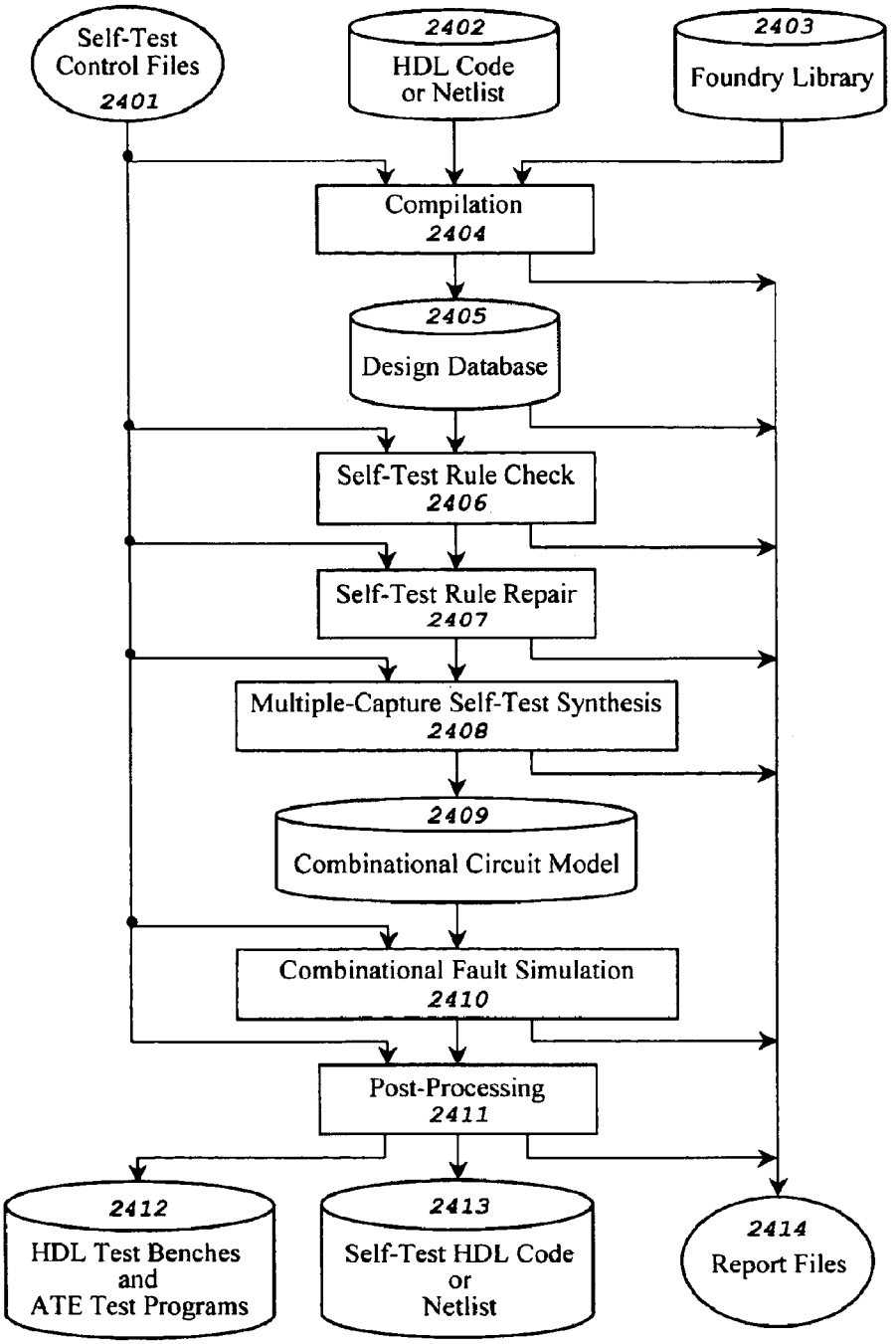

Self-Test Control Files 2401
2402 HDL Code or Netlist
2403 Foundry Library
Compilation 2404
2405 Design Database
Self-Test Rule Check 2406
Self-Test Rule Repair 2407
Multiple-Capture Self-Test Synthesis 2408
2409 Combinational Circuit Model
Combinational Fault Simulation 2410
Post-Processing 2411
2412 HDL Test Benches and ATE Test Programs
2413 Self-Test HDL Code or Netlist
2414 Report Files

FIG. 24

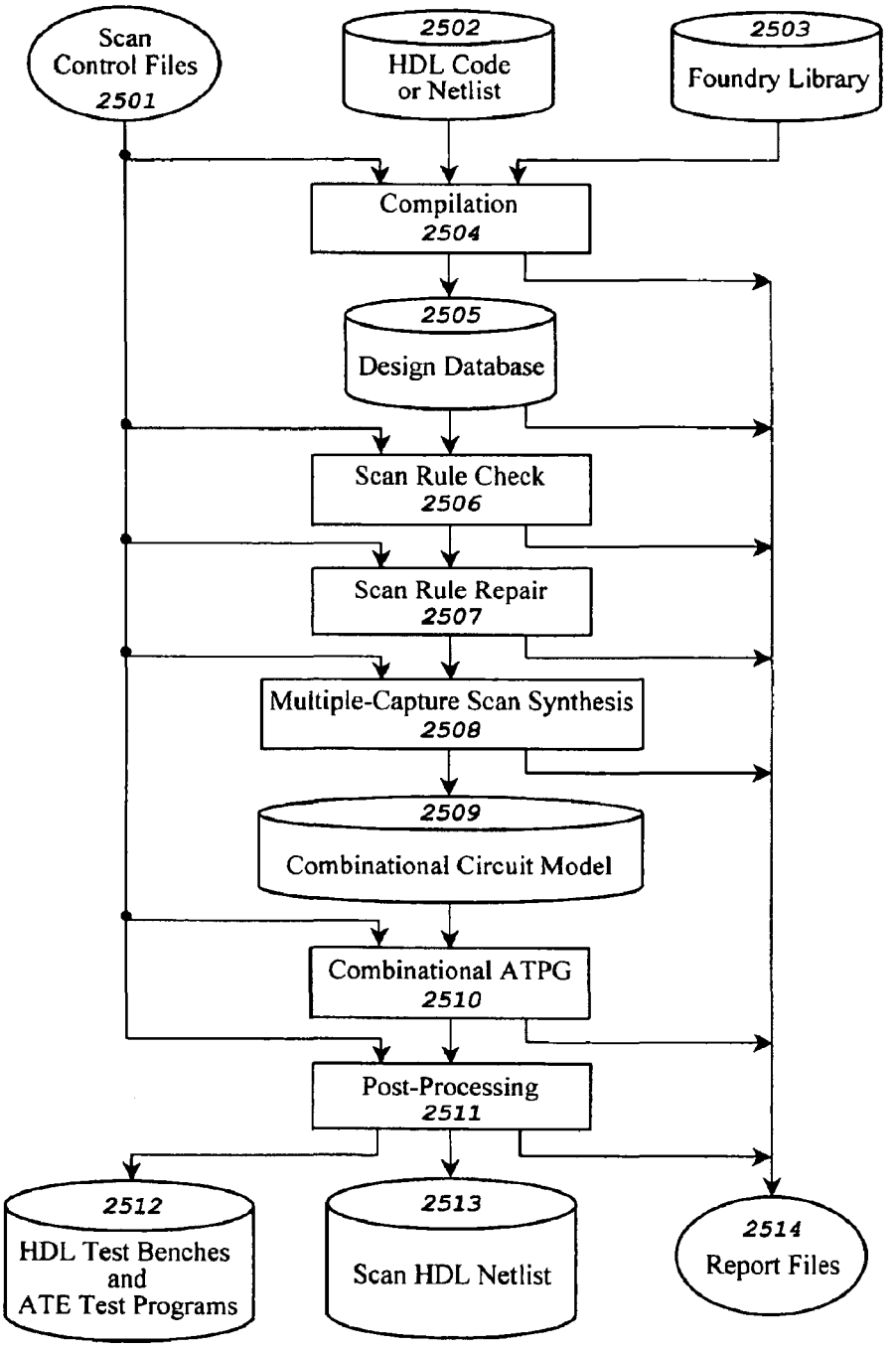

Scan Control Files 2501
2502 HDL Code or Netlist
2503 Foundry Library
Compilation 2504
2505 Design Database
Scan Rule Check 2506
Scan Rule Repair 2507
Multiple-Capture Scan Synthesis 2508
2509 Combinational Circuit Model
Combinational ATPG 2510
Post-Processing 2511
2512 HDL Test Benches and ATE Test Programs
2513 Scan HDL Netlist
2514 Report Files

FIG. 25

MULTIPLE-CAPTURE DFT SYSTEM FOR DETECTING OR LOCATING CROSSING CLOCK-DOMAIN FAULTS DURING SELF-TEST OR SCAN-TEST

RELATED APPLICATION DATA

This application claims the benefit of U.S. Provisional Application No. 60/268,601 filed Feb. 15, 2001, which is hereby incorporated by reference.

TECHNICAL FIELD

The present invention generally relates to the testing of logic designs in an integrated circuit or circuit assembly embedded with design-for-test (DFT) techniques. Specifically, the present invention relates to the detection or location of logic faults within each clock domain and logic faults crossing any two clock domains, during self-test or scan-test, in an integrated circuit or circuit assembly.

BACKGROUND OF THE INVENTION

In this specification, the term integrated circuit is used to describe a chip or MCM (multi-chip module) embedded with design-for-test (DFT) techniques. The terms circuit assembly and printed circuit board will be considered interchangeable. The term circuit assembly includes printed circuit boards as well as other types of circuit assemblies. A circuit assembly is a combination of integrated circuits. The resulting combination is manufactured to form a physical or functional unit.

An integrated circuit or circuit assembly, in general, contains two or more systems clocks, each controlling one module or logic block, called clock domain. Each system clock is either directly coming from a primary input (edge pin/connector) or generated internally. These system clocks can operate at totally unrelated frequencies (clock speeds), at sub-multiples of each other, at the same frequency but with different clock skews, or at a mix of the above. Due to clock skews among these system clocks, when a DFT technique, such as self-test or scan-test, is employed, it is very likely that faults associated with the function between two clock domains, called crossing clock-domain faults, will become difficult to test. In the worst case, these crossing clock-domain faults when propagating into the receiving clock domain could completely block detection or location of all faults within that clock domain. Thus, in order to solve the fault propagation problem, DFT approaches are proposed to take over control of all system clocks and reconfigure them as capture clocks.

Prior-art DFT approaches in this area to testing crossing clock-domain faults as well as faults within each clock domain centered on using the isolated DFT, ratio'ed DFT, and one-hot DFT techniques. They are all referred to as single-capture DFT techniques, because none of them can provide multiple skewed capture clocks (or an ordered sequence of capture clocks) in each capture cycle during self-test or scan-test.

In using the isolated DFT technique, all boundary signals crossing a clock domain and flowing into the receiving clock domains are completely blocked or disabled by forcing each of them to a predetermined logic value of 0 or 1. See U.S. Pat. No. 6,327,684 issued to Nadeau-Dostie et al. (2001). This approach, in general, can allow all clock domains to be tested in parallel. The major drawbacks of this approach are that it requires insertion of capture-disabled logic in between clock domains and all scan enable signals each associated with one clock domain must be operated at-speed. The design change could take significant efforts and it might impact normal mode operation. Running all scan enable signals at-speed requires routing them as clock signals using layout clock-tree synthesis (CTS). In addition, since boundary signals can traverse through two clock domains in both directions, this approach requires testing crossing clock-domain faults in two or more test sessions. This could substantially increase the test time required and might make the capture-disabled logic even more complex to implement than anticipated.

In using the ratio'ed DFT technique, all clock domains must be operated at sub-multiples of one reference clock. For instance, assume that a design contains 3 clock domains running at 150 MHz, 80 MHz, and 45 MHz, respectively. The 3 clock domains may have to be operated at 150 MHz, 75 MHz, and 37.5 MHz during testing. See U.S. Pat. No. 5,349,587 issued to Nadeau-Dostie et al. (1994). This approach reduces the complexity of testing a multiple-frequency design and avoids potential races or timing violations crossing clock domains. It can also allow testing of all clock domains in parallel. However, due to changes in clock-domain operating frequencies, this approach loses its self-test or scan-test intent of testing multiple-frequency designs at their rated clock speeds (at-speed) and may require significant design and layout efforts on re-timing (or synchronizing) all clock domains. Power consumption could be also another serious problem because all scan cells (memory elements) are triggered simultaneously every few cycles.

In using the one-hot DFT technique, each crossing clock-domain signal flowing into its receiving clock domains must be initialized to or held at a predetermined logic value of 0 or 1 first. This initialization is usually accomplished by shifting in predetermined logic values to all clock domains so that all crossing clock-domain signals are forced to a known state. Testing is then conducted domain-by-domain, thus, called one-hot testing. See U.S. Pat. No. 5,680,543 issued to Bhawmik et al. (1997). The major benefits of using this approach are that it can still detect or locate crossing clock-domain faults and does not need insertion of disabled logic, in particular, in critical paths crossing clock domains. However, unlike the isolated or ratio'ed DFT approach, this approach requires testing of all clock domains in series, resulting in long test time. It also requires significant design and layout efforts on re-timing (or synchronizing) all clock domains.

Two additional prior-art DFT approaches had also been proposed, one for scan-test, the other for self-test. Both approaches are referred to as multiple-capture DFT techniques, because they can provide multiple skewed capture clocks (or an ordered sequence of capture clocks) in each capture cycle during scan-test or self-test.

The first prior-art multiple-capture DFT approach is to test faults within each clock domain and faults between two clock domains in scan-test mode. See U.S. Pat. No. 6,070,260 issued to Buch et al. (2000) and U.S. Pat. No. 6,195,776 issued to Ruiz et al. (2001). These approaches rest on using multiple skewed scan clocks or multiple skew capture events each operating at the same reduced clock speed in an ATE (automatic test equipment) to detect faults. Combinational ATPG (automatic test pattern generation) is used to generate scan-test patterns and ATE test programs are created to detect faults in the integrated circuit. Unfortunately, currently available ATPG tools only assume the application of one clock pulse (clock cycle) to each clock domain. Thus, these approaches can only detect stuck-at faults in scan-test

mode. No prior art using multiple skewed capture clocks were proposed to test delay or stuck-at faults requiring two or more capture clock pulses for full-scan or partial-scan designs.

The second prior-art multiple-capture DFT approach is to test faults within each clock domain and faults between two clock domains in self-test mode. See the paper co-authored by Hetherington et al. (1999). This approach rests on using multiple shift-followed-by-capture clocks each operating at its operating frequency, in a programmable capture window, to detect faults at-speed. It requires clock suppression, complex scan enable (SE) timing waveforms, and shift clock pulses in the capture window to control the capture operation. These shift clock pulses may also need precise timing alignment. As a result, it becomes quite difficult to perform at-speed self-test for designs containing clock domains operated at totally unrelated frequencies, e.g., 133 MHz and 60 MHz.

Thus, there is a need for an improved method, apparatus, or computer-aided design (CAD) system that allows at-speed or slow-speed testing of faults within clock domains and between any two clock domains using a simple multiple-capture DFT technique. The method and apparatus of the present invention will control the multiple-capture operations of the capture clocks in self-test or scan-test mode. It does not require using shift clock pulses in the capture window, inserting capture-disabled logic in normal mode, applying clock suppression on capture clock pulses, and programming complex timing waveforms on scan enable (SE) signals. In addition, the CAD system of the present invention further comprises the computer-implemented steps of performing multiple-capture self-test or scan synthesis, combinational fault simulation, and combinational ATPG that are currently unavailable in the CAD field using multiple-capture DFT techniques.

SUMMARY OF THE INVENTION

Accordingly, a primary objective of the present invention is to provide an improved multiple-capture DFT system implementing the multiple-capture DFT technique. Such a DFT system will comprise a method or apparatus for allowing at-speed/slow-speed detection or location of faults within all clock domains and faults crossing clock domains in an integrated circuit or circuit assembly. In the present invention, the method or apparatus can be realized and placed inside or external to the integrated circuit or circuit assembly.

A computer-aided design (CAD) system that synthesizes such a DFT system and generates desired HDL test benches and ATE test programs is also included in the present invention. A hardware description language (HDL) is used to represent the integrated circuit includes, but is not limited to, Verilog or VHDL. An ATE is an IC tester or any equipment that realizes the multiple-capture DFT system and is external to the integrated circuit or circuit assembly under test.

The present invention focuses on multiple-capture DFT systems for self-test and scan-test. In a self-test environment, a self-test cycle often comprises 3 major operations: shift, capture, and compact. The shift and compact operations can occur concurrently during each self-test cycle. In order to increase the circuit's fault coverage, it is often necessary to include scan-test cycles to perform top-up ATPG. A scan-test cycle often comprises 3 major operations in a scan-test environment: shift, capture, and compare. The shift and compare operations can occur concurrently during each scan-test cycle. In a mixed self-test and scan-test environment, the scan-test cycle may execute a compact operation rather than the compare operation. Thus, in the present invention, a self-test cycle further comprises the shift, capture, and compare operations, and a scan-test cycle further comprises the shift, capture, and compact operations.

The multiple-capture DFT system of the present invention further comprises any method or apparatus for executing the shift and compact or shift and compare operations concurrently during each self-test or scan-test cycle. It is applicable to test any integrated circuit or circuit assembly which contains N clock domains, where N>1. Each capture clock controls one clock domain and can operate at its rated clock speed (at-speed) or at a reduced clock speed (slow-speed), when desired.

During the shift operation, the multiple-capture DFT system first generates and shifts in (loads) N pseudorandom or predetermined stimuli to all scan cells within all clock domains, concurrently. The shifting frequency is irrelevant to at-speed testing. Depending on needs, a slower frequency can be used to reduce power consumption and a faster frequency can be used to reduce the test application time. The multiple-capture DFT system must wait until all stimuli have been loaded or shifted into all scan cells. By that time, all scan enable (SE) signals each associated with one clock domain shall switch from the shift operation to the capture operation. After the capture operation is completed, all scan enable (SE) signals shall switch from the capture operation to the shift operation. One global scan enable (GSE) signal can be simply used to drive these scan enable signals.

The multiple-capture DFT system of the present invention further comprises any method or apparatus for performing the shift operation at any selected clock speed within each clock domain and using only one global scan enable (GSE) signal to drive all scan enable (SE) signals for at-speed or slow-speed testing. The GSE signal can be also operated at its selected reduced clock speed. Thus, there is no need to route these SE signals as clock signals using layout clock tree synthesis (CTS). This invention applies to any self-test or scan-test method that requires multiple capture clock pulses (without including shift clock pulses) in the capture cycle.

After the shift operation is completed, an ordered sequence of capture clocks is applied to all clock domains. During the capture operation, each ordered sequence contains N capture clocks of which only one or a few will be active at one time. There are no shift clock pulses present within each capture cycle. Testing of delay faults at-speed is now performed by applying two consecutive capture clock pulses (double captures) rather than using the shift-followed-by-capture clock pulses. Performing multiple captures in the capture cycle reduces the risk of delay test invalidation and false paths that might occur due to illegal states in scan cells resulting from filling them with pseudorandom or predetermined stimuli.

In the present invention, the multiple-capture DFT system uses a daisy-chain clock-triggering or token-ring clock-enabling technique to generate and order capture clocks one after the other. One major benefit of using this approach is that the test results are repeatable no matter what clock speed will be used for each capture clock. The problem is it could be difficult to precisely control the relative clock delay between two adjacent capture clocks for testing delay faults between clock domains.

As an example, assume that the capture cycle contains 4 capture clocks, CK**1**, CK**2**, CK**3**, and CK**4**. (Please refer to

FIGS. 3 and 10 in the DETAILED DESCRIPTION OF THE DRAWINGS section for further descriptions). The daisy-chain clock-triggering technique implies that completion of the shift cycle triggers the GSE signal to switch from shift to capture cycle which in turn triggers CK1, the rising edge of the last CK1 pulse triggers CK2, the rising edge of the last CK2 pulse triggers CK3, and the rising edge of the last CK3 pulse triggers CK4. Finally, the rising edge of the last CK4 pulse triggers the GSE signal to switch from capture to shift cycle.

The token-ring clock-enabling technique implies that completion of the shift cycle enables the GSE signal to switch from shift to capture cycle which in turn enables CK1, completion of CK1 pulses enables CK2, completion of CK2 pulses enables CK3, and completion of CK3 pulses enables CK4. Finally, completion of CK4 pulses enables the GSE signal to switch from capture to shift cycle.

The only difference between these two techniques is that the former uses clock edges to trigger the next operation, the latter uses signal levels to enable the next operation. In practice, a mixed approach can be employed. Since a daisy-chain or token-ring approach is used, the multiple-capture DFT system allows testing of any frequency domain at a reduced clock speed when this particular frequency domain cannot operate at-speed. This is very common in testing high-speed integrated circuits, such as microprocessors and networking chips, where different clock speeds of chips are sold at different prices. In addition, due to its ease of control, this approach further allows at-speed scan-test simply using internally reconfigured capture clocks. Thus, a low-cost tester (ATE) can be used for at-speed scan-test, in addition to at-speed self-test.

The multiple-capture DFT system in the present invention further comprises applying an ordered sequence of capture clocks and operating each capture clock at its selected clock speed in the capture operation (cycle). The ordered sequence of capture clocks is applied to the circuit under test one-by-one using the daisy-chain clock-triggering or token-ring clock-enabling technique. The order of these capture clocks is further programmable, when it's required to increase the circuit's fault coverage. Each capture clock can be also disabled or chosen to facilitate fault diagnosis. In addition, when two clock domains do not interact with each other, they can be tested simultaneously to shorten the capture cycle time.

Each capture clock of the present invention further comprises one or more clock pulses. The number of clock pulses is further programmable. When self-test is employed, the multiple-capture DFT system is usually placed inside the integrated circuit and, thus, all capture clocks are generated internally. When scan-test is employed, the multiple-capture DFT system is usually resided in an ATE and, thus, all capture clocks are controlled externally. However, for at-speed scan-test, it's often required to capture output responses using its respective operating frequency within each clock domain. The present invention further comprises any method or apparatus for allowing use of internally-generated or externally-controlled capture clocks for at-speed scan-test or self-test.

After the capture operation is completed, all output responses captured at all scan cells are compacted internally to signatures or shifted out to the multiple-capture DFT system for direct comparison. The compact or compare operation occurs concurrently with the shift operation, and the process of shift, capture, and compact/compare operations shall continue until a predetermined limiting criteria, such as completion of all self-test or scan-test cycles, is reached. Finally, the multiple-capture DFT system will compare the signatures against expected signatures when the compact operation is employed during self-test or scan-test. Such comparison can be done either in the integrated circuit with a built-in comparator or in an ATE by shifting the final signatures out for analysis.

In the present invention, both self-test and scan-test techniques are employed to detect or locate stuck-at and delay faults. The stuck-at faults further comprise other stuck-type faults, such as open and bridging faults. The delay faults further comprise other non-stuck-type delay faults, such as transition (gate-delay), multiple-cycle delay, and path-delay faults. In addition, each scan cell can be a multiplexed D flip-flop or a level sensitive latch, and the integrated circuit or circuit assembly under test can be a full-scan or partial-scan design.

In general, it is only required to apply one clock pulse and two consecutive clock pulses to test stuck-at faults and delay faults within one clock domain, respectively. Multiple-cycle paths present within one clock domain and between clock domains, however, require waiting for a number of clock cycles for capturing. To test multiple-cycle paths within clock domains, the present invention further comprise applying only one clock pulse to test these multiple-cycle paths within each clock domain by reducing the frequency of that domain's capture clock speed to the level where only paths of equal cycle latency (cycle delays) are captured at its intended rated clock speed one at a time. To test multiple-cycle paths between two clock domains, the present invention further comprise adjusting the relative clock delay along the paths to the level where the crossing-boundary multiple-cycle paths are captured at its intended rated clock speed.

To summarize, the present invention centers on using one global scan enable (GSE) signal for driving all scan enable (SE) signals at a reduced clock speed and applying an ordered sequence of capture clocks for capturing output responses in both self-test and scan-test modes. The present invention assumes that the integrated circuit or circuit assembly must contain two or more clock domains each controlled by one capture clock. During self-test, each capture clock shall contain one or more clock pulses, and during scan-test, one of the capture clocks must contain two or more clock pulses.

Due to its ease of control on the scan enable and capture clock signals, the multiple-capture DFT system of the present invention can now be easily realized by an apparatus and synthesized using computer-aided design (CAD) tools. The present invention further comprises such a CAD system for synthesizing the apparatus and verifying its correctness using combinational fault simulation and combinational ATPG in self-test or scan-test mode.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, advantages and features of the invention will become more apparent when considered with the following specification and accompanying drawings wherein:

FIG. 1 shows an example full-scan or partial-scan design with 4 clock domains and 4 system clocks, where a multiple-capture DFT system in accordance with the present invention is used to detect or locate stuck-at faults at a reduced clock speed in self-test or scan-test mode.

FIG. 2 shows a multiple-capture DFT system with multiple PRPG-MISR pairs, in accordance with the present invention, which is used at a reduced clock speed in self-test mode to detect or locate stuck-at faults in the design given in FIG. 1.

FIG. **3** shows a timing diagram of the full-scan design given in FIG. **1**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and stuck-at faults crossing clock domains in self-test mode. The chain of control events is also shown.

FIG. **4** shows a timing diagram of the full-scan design given in FIG. **1**, in accordance with the present invention, where a shortened yet ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and stuck-at faults crossing clock domains in self-test mode.

FIG. **5** shows a timing diagram of the full-scan design given in FIG. **1**, in accordance with the present invention, where an expanded yet ordered sequence of capture clocks is used to detect or locate other stuck-type faults within each clock domain and other stuck-type faults crossing clock domains in self-test or scan-test mode.

FIG. **6** shows a timing diagram of the partial-scan design given in FIG. **1**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **7** shows an example full-scan or partial-scan design with 4 clock domains and 4 system clocks, where a multiple-capture DFT system in accordance with the present invention is used to detect or locate stuck-at, delay, and multiple-cycle delay faults at its desired clock speed in self-test or scan-test mode.

FIG. **8** shows a multiple-capture DFT system with multiple PRPG-MISR pairs, in accordance with the present invention, which is used at its desired clock speed in self-test or scan-test mode to detect or locate stuck-at, delay, and multiple-cycle delay faults in the design given in FIG. **7**.

FIG. **9** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and stuck-at faults crossing clock domains in self-test mode.

FIG. **10** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode. The chain of control events is also shown.

FIG. **11** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where a shortened yet ordered sequence of capture clocks is used to detect or locate delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **12** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and delay faults crossing clock domains in self-test or scan-test mode.

FIG. **13** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate delay faults within each clock domain and delay faults crossing clock domains in self-test or scan-test mode.

FIG. **14** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where a reordered sequence of capture clocks is used to detect or locate delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **15** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an expanded yet ordered sequence of capture clocks is used to detect or locate additional delay faults within each clock domain and additional stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **16** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate 2-cycle delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **17** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate 2-cycle delay faults within each clock domain and 2-cycle delay faults crossing clock domains in self-test or scan-test mode.

FIG. **18** shows a timing diagram of the partial-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **19** shows a timing diagram of the partial-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **20** shows a timing diagram of the partial-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate 2-cycle delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **21** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where the capture clock CK**2** during the capture cycle is chosen to diagnose faults captured by CK**2** in self-test or scan-test mode.

FIG. **22** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where the capture clocks CK**1** and CK**3** during the capture cycle are chosen to diagnose faults captured by CK**1** and CK**3** in self-test or scan-test mode.

FIG. **23** shows a timing diagram of the full-scan design given in FIG. **1**, in accordance with the present invention, where all capture clocks during the shift cycle are skewed to reduce power consumption.

FIG. **24** shows a multiple-capture CAD system in accordance with the present invention, where a CAD system is used to implement the multiple-capture DFT technique on a full-scan or partial-scan design in self-test mode.

FIG. **25** shows a multiple-capture CAD system in accordance with the present invention, where a CAD system is used to implement the multiple-capture DFT technique on a full-scan or partial-scan design in scan-test mode.

DETAILED DESCRIPTION OF THE DRAWINGS

The following description is of presently contemplated as the best mode of carrying out the present invention. This

description is not to be taken in a limiting sense but is made merely for the purpose of describing the principles of the invention. The scope of the invention should be determined by referring to the appended claims.

FIG. **1** shows an example full-scan or partial-scan design with a multiple-capture DFT system, of one embodiment of the invention. The design **133** contains 4 clock domains, CD**1** **102** to CD**4** **105**, and 4 system clocks, CK**1** **111** to CK**4** **120**. Each system clock controls one clock domain. CD**1** **102** and CD**2** **103** talk to each other via a crossing clock-domain logic block CCD**1** **106**; CD**2** **103** and CD**3** **104** talk to each other via a crossing clock-domain logic block CCD**2** **107**; and CD**3** **104** and CD**4** **105** talk to each other via a crossing clock-domain logic block CCD**3** **108**.

The 4 clock domains, CD**1** **102** to CD**4** **105**, are originally designed to run at 150 MHz, 100 MHz, 100 MHz, and 66 MHz, respectively. However, in this example, since a DFT (self-test or scan-test) technique is only employed to detect or locate stuck-at faults in the design **133**, all system clocks, CK**1** **111** to CK**4** **120**, are reconfigured to operate at 10 MHz. The reconfigured system clocks are called capture clocks.

During self-test or scan-test, the multiple-capture DFT system **101** will take over the control of all stimuli, **109**, **112**, **115**, and **118**, all system clocks, CK**1** **111** to CK**4** **120**, and all output responses, **110**, **113**, **116**, and **119**.

During the shift operation, the multiple-capture DFT system **101** first generates and shifts pseudorandom or predetermined stimuli through **109**, **112**, **115**, and **118** to all scan cells SC in all scan chains SCN within the 4 clock domains, CD**1** **102** to CD**4** **105**, simultaneously. The multiple-capture DFT system **101** shall wait until all stimuli, **109**, **112**, **115**, and **118**, have been shifted into all scan cells SC. It should be noted that, during the shift operation, the capture clock can be operated either at its rated clock speed (at-speed) or at a desired clock speed.

After the shift operation is completed, an ordered sequence of capture clocks is applied to all clock domains, CD**1** **102** to CD**4** **105**. During the capture operation, each capture clock can operate at its rated clock speed (at-speed) or at a reduced speed (slow-speed), and can be generated internally or controlled externally. In this example, all system clocks, CK**1** **111** to CK**4** **120**, are reconfigured to operate at a reduced frequency of 10 MHz.

After the capture operation is completed, the output responses captured at all scan cells SC are shifted out through responses **110**, **113**, **116**, and **119** to the multiple-capture DFT system **101** for compaction during the compact operation or direct comparison during the compare operation.

Based on FIG. **1**, the timing diagrams given in FIGS. **3** to **6** are used to illustrate that, by properly ordering the sequence of capture clocks and by adjusting relative inter-clock delays, stuck-at faults within each clock domain and crossing clock domains can be detected or located in self-test or scan-test mode. Please note that different ways of ordering the sequence of capture clocks and adjusting relative inter-clock delays will result in different faults to be detected or located.

FIG. **2** shows a multiple-capture DFT system with three PRPG-MISR pairs, of one embodiment of the invention, used to detect or locate stuck-at faults in the design **133** given in FIG. **1** in self-test mode.

Pseudorandom pattern generators (PRPGs), **211** to **213**, are used to generate pseudorandom patterns. Phase shifters, **214** to **216**, are used to break the dependency between different outputs of the PRPGS. The bit streams coming from the phase shifters become test stimuli, **109**, **112**, **115**, and **118**.

Space compactors, **217** to **219**, are used to reduce the number of bit streams in test responses, **110**, **113**, **116**, and **119** shifted out of CD**1** **102**, CD**2** **103**, CD**3** **104**, and CD**4** **105**, respectively. Space compactors are optional and are only used when the overhead of a MISR becomes a concern. The outputs of the space compactors are then compressed by multiple input signature registers (MISRs), **220** to **222**. The contents of MISRs after all test stimuli are applied become signatures, **236** to **238**. The signatures are then be compared by comparators, **223** to **225**, with corresponding expected values. The error indicator **226** is used to combine the individual pass/fail signals, **242** to **244**, a global pass/fail signal **245**. Alternatively, the signatures in MISRs **220** to **222** can be shifted to the outside of the design for comparison through a single scan chain composed of elements **223**, **239**, **224**, **240**, **225**, and **241**.

The central self-test controller **202** controls the whole test process by manipulating individual scan enable signals, **204** to **207**, and by reconfiguring capture clocks, CK**1** **111** to CK**4** **120**. Especially, the scan enable signals, **204** to **207**, can be controlled by one global scan enable signal GSE **201**, which can be a slow signal in that it does not have to settle down in half of the cycle of any clock applied to any clock domain. Some additional control signals **203**, connected to **208**, **209** and **210**, are needed to conduct other control tasks.

The clock domains **103** and **104**, which are operated at the same frequency, share the same pair of PRPG **212** and MISR **221**. It should be noted that the skew between the clocks CK**2** **114** and CK**3** **117** should be properly managed to prevent any timing violations during the shift operation and any races during the capture operation.

All storage elements in PRPGs, **211** to **213**, and MISRs, **220** to **222**, can be connected into a scan chain through paths **246** to **252** from which predetermined patterns can be shifted in for reseeding and computed signatures can be shifted out for analysis. This configuration helps in increasing fault coverage and in facilitating fault diagnosis.

FIG. **3** shows a timing diagram of a full-scan design given in FIG. **1**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test mode. The timing diagram **300** shows the sequence of waveforms of the 4 capture clocks, CK**1** **111** to CK**4** **120**, operating at the same frequency.

During each shift cycle **310**, a series of pulses of 10 MHz are applied through capture clocks, CK**1** **111** to CK**4** **120**, to shift stimuli to all scan cells within all clock domains, CD**1** **102** to CD**4** **105**.

During each capture cycle **311**, 4 sets of capture clock pulses are applied in the following order: First, one capture pulse is applied to CK**1** **111** to detect or locate stuck-at faults within the clock domain CD**1** **102**. Second, one capture pulse is applied to CK**2** **114** to detect or locate stuck-at faults within the clock domain CD**2** **103**. Third, one capture pulse is applied to CK**3** **117** to detect or locate stuck-at faults within the clock domain CD**3** **104**. Fourth, one capture pulse is applied to CK**4** **120** to detect or locate stuck-at faults within the clock domain CD**4** **105**.

In addition, the stuck-at faults which can be reached from lines **121**, **125**, and **129** in the crossing clock-domain logic blocks CCD**1** **106** to CCD**3** **108**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **307** between the rising edge of the capture pulse of CK**1** **111** and the rising edge of the capture pulse of CK**2** **114** must be adjusted so that no

races or timing violations would occur while the output responses **123** are captured through the crossing clock-domain logic block CCD**1** **106**.

The same principle applies to the relative clock delay **308** between CK**2** **114** and CK**3** **117**, and the relative clock delay **309** between CK**3** **117** and CK**4** **120** for capturing output responses, **127** and **131**, through CCD**2** **107** and CCD**3** **108**, respectively.

It should be noticed that, generally, during each shift cycle, any capture clock is allowed to operate at its desired or a reduced clock speed. In addition, it is not necessary that all capture clocks must operate at the same clock speed. Furthermore, to reduce peak power consumption during the shift cycle, all capture clocks can be skewed so that at any given time only scan cells within one clock domain can change states. One global scan enable signal GSE **201**, operated at a reduced clock speed, can also be used, when requested, to switch the test operation from the shift cycle to the capture cycle, and vice versa.

The daisy-chain clock-triggering technique is used to generate and order the sequence of capture clocks one after the other in the following way: The rising edge of the last pulse in the shift cycle triggers the event **301** of applying 0 to the global scan enable GSE **201**, switching the test operation from the shift cycle to the capture cycle. The falling edge of GSE **201** triggers the event **302** of applying one capture pulse to CK**1** **111**. Similarly, the rising edge of the capture pulse of CK**1** **111** triggers the event **303** of applying one capture pulse to CK**2** **114**, the rising edge of the capture pulse of CK**2** **114** triggers the event **304** of applying one capture pulse to CK**3** **117**, and the rising edge of the capture pulse of CK**3** **117** triggers the event **305** of applying one capture pulse to CK**4** **120**. Finally, the rising edge of the capture pulse of CK**4** **120** triggers the event **306** of applying 1 to the global scan enable GSE **201**, switching the test operation from the capture cycle to the shift cycle. This daisy-chain clock-triggering technique is also used to order the sequence of capture clocks in FIGS. **4** to **6**.

FIG. **4** shows a timing diagram of a full-scan design given in FIG. **1**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with a shortened yet ordered sequence of capture clocks in self-test mode. The timing diagram **400** shows the sequence of waveforms of the 4 capture clocks, CK**1** **111** to CK**4** **120**, operating at the same frequency.

During each shift cycle **402**, a series of clock pulses of 10 MHz are applied through capture clocks, CK**1** **111** to CK**4** **120**, to shift stimuli to all scan cells within all clock domains, CD**1** **102** to CD**4** **105**.

During each capture cycle **403**, two sets of capture clock pulses are applied in the following order: First, one capture pulse is applied to CK**1** **111** and CK**3** **117** simultaneously to detect or locate stuck-at faults within the clock domain CD**1** **102** and CD**3** **104**, respectively. Second, one capture pulse is applied to CK**2** **114** and CK**4** **120** simultaneously to detect or locate stuck-at faults within the clock domain CD**2** **103** and CD**4** **105**, respectively.

In addition, the stuck-at faults which can be reached from lines **121**, **128**, and **129** in the crossing clock-domain logic blocks CCD**1** **106** to CCD**3** **108**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **401** between the rising edge of the capture pulse for CK**1** **111** and CK**3** **117** and the rising edge of the capture pulse for CK**2** **114** and CK**4** **120**, must be adjusted so that no races or timing violations would occur while the output responses, **123**, **126**, and **131**, are captured through the crossing clock-domain logic blocks CCD**1** **106** to CCD**3** **108**.

FIG. **5** shows a timing diagram of a full-scan design in FIG. **1** of one embodiment of the invention for detecting or locating other stuck-type faults within each clock domain and other stuck-type faults crossing clock domains with an expanded yet ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **500** shows the sequence of waveforms of the 4 capture clocks, CK**1** **111** to CK**4** **120**, operating at the same frequency.

During each shift cycle **503**, a series of clock pulses of 10 MHz are applied through capture clocks, CK**1** **111** to CK**4** **120**, to shift stimuli to all scan cells within all clock domains, CD**1** **102** to CD**4** **105**.

During each capture cycle **504**, two sets of capture clock pulses are applied in the following order: First, two capture pulses are applied to CK**1** **111** and CK**3** **117**, simultaneously. Second, one capture pulse is applied to CK**2** **114** and CK**4** **120**, simultaneously. Stuck-at faults in all crossing clock-domain combinations, from **121** to **123**, from **124** to **122**, from **125** to **127**, from **128** to **126**, from **129** to **131**, from **132** to **130**, can be detected or located if the following condition is satisfied: The relative clock delay **501** between the rising edge of the first capture pulse of CK**1** **111** and CK**3** **117** and the rising edge of the capture pulse of CK**2** **114** and CK**4** **120** must be adjusted so that no races or timing violations would occur while the output responses **123**, **126**, and **131** are captured through the crossing clock-domain logic block CCD**1** **106** to CCD**3** **108**, respectively. The relative clock delay **502** between the rising edge of the capture pulse of CK**2** **114** and CK**4** **120** and the second capture pulse of CK**1** **111** and CK**3** **117** must be adjusted so that no races or timing violations would occur while the output responses **122**, **127**, and **130** are captured through the crossing clock-domain logic block CCD**1** **106** to CCD**3** **108**, respectively.

FIG. **6** shows a timing diagram of a feed-forward partial-scan design given in FIG. **1**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with a shortened yet ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that the clock domains CD**1** **102** to CD**4** **105** contain a number of un-scanned storage cells that form a sequential depth of no more than 2. The timing diagram shows the sequence of waveforms of the 4 capture clocks, CK**1** **111** to CK**4** **120**, operating at the same frequency.

During each shift cycle **606**, a series of clock pulses of 10 MHz are applied through capture clocks, CK**1** **111** to CK**4** **120**, to shift stimuli to all scan cells within all clock domains, CD**1** **102** to CD**4** **105**.

During each capture cycle **607** which extends through the intervals **601** to **605**, two sets of capture clock pulses are applied in the following order: First, three pulses of 10 MHz, two being functional pulses and one being a capture pulse, are applied to CK**1** **111** and CK**3** **117** simultaneously to detect or locate stuck-at faults within the clock domain CD**1** **102** and CD**3** **104**, respectively. Second, three pulses of 10 MHz, two being functional pulses and one being a capture pulse, are applied to CK**2** **114** and CK**4** **120** simultaneously to detect or locate stuck-at faults within the clock domain CD**2** **103** and CD**4** **105**, respectively.

In addition, the stuck-at faults which can be reached from lines **121**, **128**, and **129** in the crossing clock-domain logic blocks CCD**1** **106** to CCD**3** **108**, respectively, are also detected or located simultaneously if the following condition

is satisfied: The relative clock delay **603** between the rising edge of the capture pulse for CK1 **111** and CK3 **117** and the rising edge of the capture pulse for CK2 **114** and CK4 **120** must be adjusted so that no races or timing violations would occur while the output responses, **123**, **126**, and **131**, are captured through the crossing clock-domain logic blocks CCD1 **106** to CCD3 **108**.

FIG. **7** shows an example full-scan or partial-scan design with a multiple-capture DFT system **701**, of one embodiment of the invention. The design **733** is the same as the design **133** given in FIG. **1**. Same as in FIG. **1**, the 4 clock domains, CD1 **702** to CD4 **705**, are originally designed to run at 150 MHz, 100 MHz, 100 MHz, and 66 MHz, respectively. The only difference from FIG. **1** is that these clock frequencies will be used directly without alternation in order to implement at-speed self-test or scan-test for stuck-at, delay, and multiple-cycle delay faults within each clock domain and crossing clock domains. In self-test or scan-test mode, the multiple-capture DFT system **701** will take over the control of all stimuli, **709**, **712**, **715** and **718**, all system clocks, CK1 **711** to CK4 **720**, and all output responses, **710**, **713**, **716** and **719**.

Based on FIG. **7**, the timing diagrams given in FIGS. **9** to **20** are used to illustrate that, by properly ordering the sequence of capture pulses and by adjusting relative inter-clock delays, the at-speed detection or location of stuck-at, delay, and multiple-cycle delay faults within each clock domain and crossing clock domains can be achieved in self-test or scan-test mode. Please note that different ways of ordering the sequence of capture pulses and adjusting relative inter-clock delays will result in different faults to be detected or located.

FIG. **8** shows a multiple-capture DFT system with three PRPG-MISR pairs, of one embodiment of the invention, used in self-test or scan-test mode to detect or locate stuck-at, delay, and multiple-cycle delay faults in the design given in FIG. **7**. The composition and operation of the multiple-capture DFT system is basically the same as the one given in FIG. **2**. There are two major differences: One is that, in this example, the original clock frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are used directly without alternation in order to implement at-speed self-test or scan-test. The other is that more care needs to be taken in the physical design of scan chains, etc., in this example.

The clock domains **703** and **704**, which are operated at the same frequency, share the same pair of PRPG **812** and MISR **821**. It should be noted that the skew between the clocks CK2 **714** and CK3 **717** should be properly managed to prevent any timing violations during the shift operation and any races during the capture operation.

All storage elements in PRPGs, **811** to **813**, and MISRs, **820** to **822**, can be connected into a scan chain from which predetermined patterns can be shifted in for reseeding and computed signatures can be shifted out for analysis. This configuration helps in increasing fault coverage and in facilitating fault diagnosis.

FIG. **9** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test mode. The timing diagram **900** shows the sequence of waveforms of the 4 capture clocks, CK1 **711** to CK4 **720**, operating at different frequencies. This timing diagram is basically the same as the one given in FIG. **3** except the capture clocks, CK1 **711** to CK4 **720**, run at 150 MHz, 100 MHz, 100 MHz, and 66 MHz, respectively, in both shift and capture cycles, instead of 10 MHz as in FIG. **3**.

FIG. **10** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating delay faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1000** shows the sequence of waveforms of the 4 capture clocks, CK1 **711** to CK4 **720**, operating at different frequencies.

During each shift cycle **1014**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK1 **711** to CK4 **720**, to shift stimuli to all scan cells within all clock domains, CD1 **702** to CD4 **705**.

During each capture cycle **1015**, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of 150 MHz are applied to CK1 **711** to detect or locate delay faults within the clock domain CD1 **702**. Second, two capture pulses of 100 MHz are applied to CK2 **714** to detect or locate delay faults within the clock domain CD2 **703**. Third, two capture pulses of 100 MHz are applied to CK3 **717** to detect or locate delay faults within the clock domain CD3 **704**. Fourth, two capture pulses of 66 MHz are applied to CK4 **720** to detect or locate delay faults within the clock domain CD4 **705**.

In addition, the stuck-at faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD1 **706** to CCD3 **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1008** between the rising edge of the second capture pulse of CK1 **711** and the rising edge of the first capture pulse of CK2 **714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCD1 **706**.

The same principle applies to the relative clock delay **1010** between CK2 **714** and CK3 **717**, and the relative clock delay **1012** between CK3 **717** and CK4 **720** for capturing the output responses, **727** and **731**, through CCD2 **707** and CCD3 **708**, respectively.

The daisy-chain clock-triggering technique is used to generate and order the sequence of capture clocks one after the other in the following way: The rising edge of the last pulse in the shift cycle triggers the event **1001** of applying 0 to the global scan enable GSE **801**, switching the test operation from the shift cycle to the capture cycle. The falling edge of GSE **801** triggers the event **1002** of applying two capture pulses to CK1 **711**. Similarly, the rising edge of the second capture pulse of CK1 **711** triggers the event **1003** of applying two capture pulses to CK2 **714**, the rising edge of the second capture pulse of CK2 **714** triggers the event **1004** of applying two capture pulses to CK3 **717**, and the rising edge of the second capture pulse of CK3 **717** triggers the event **1005** of applying two capture pulses to CK4 **720**. Finally, the rising edge of the second capture pulse of CK4 **720** triggers the event **1006** of applying 1 to the global scan enable GSE **801**, switching the test operation from the capture cycle to the shift cycle. This daisy-chain clock-triggering technique is also used to order the sequence of capture clocks in FIG. **9** and FIGS. **11** to **20**.

FIG. **11** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating delay faults within each clock domain and stuck-at faults crossing clock domains with a shortened yet ordered sequence of capture clocks in self-test or scan-

test mode. The timing diagram **1100** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1108**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1109**, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of frequency 150 MHz are applied to CK**1** **711** and two clock pulses of frequency 100 MHz are applied to CK**3** **717**, simultaneously, to detect or locate delay faults within the clock domain CD**1** **702** and CD**3** **704**, respectively. Second, two capture pulses of frequency 100 MHz are applied to CK**2** **714** and two capture pulses of frequency 66 MHz are applied to CK**4** **720**, simultaneously, to detect or locate delay faults within the clock domain CD**2** **703** and CD**4** **705**, respectively.

In addition, the stuck-at faults which can be reached from lines **721**, **728**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1102** between the rising edge of the second capture pulse of CK**1** **711** and the rising edge of the first capture pulse of CK**2** **714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCD**1** **706**.

The same principle applies to the relative clock delay **1104** between CK**3** **717** and CK**2** **714**, and the relative clock delay **1106** between CK**3** **717** and CK**4** **720** for capturing the output responses, **726** and **731**, through CCD**2** **707** and CCD**3** **708**, respectively.

FIG. **12** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and delay faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1200** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1204**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1205**, 4 sets of capture clock pulses are applied in the following order: First, one capture pulse of 150 MHz is applied to CK**1** **711** to detect or locate stuck-at faults within the clock domain CD**1** **702**. Second, one capture pulse of 100 MHz is applied to CK**2** **714** to detect or locate stuck-at faults within the clock domain CD**2** **703**. Third, one capture pulse of 100 MHz is applied to CK**3** **717** to detect or locate stuck-at faults within the clock domain CD**3** **704**. Fourth, one capture pulse of 66 MHz is applied to CK**4** **720** to detect or locate stuck-at faults within the clock domain CD**4** **705**.

In addition, the delay faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delays **1201** between the rising edge of the capture pulse of CK**1** **711** and the rising edge of the capture pulse of CK**2** **714** must be adjusted to meet the at-speed timing requirements for paths from **721** to **723**. Similarly, the relative clock delay **1202** between CK**2** **714** and CK**3** **717**, and the relative clock delay **1203** between CK**3** **717** and CK**4** **720**, must be adjusted to meet the at-speed timing requirements for paths from **725** to **727**, and paths from **729** to **731**, respectively.

FIG. **13** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating delay faults within each clock domain and delay faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1300** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1308**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1309**, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of 150 MHz are applied to CK**1** **711** to detect or locate delay faults within the clock domain CD**1** **702**. Second, two capture pulses of 100 MHz are applied to CK**2** **714** to detect or locate delay faults within the clock domain CD**2** **703**. Third, two capture pulses of 100 MHz are applied to CK**3** **717** to detect or locate delay faults within the clock domain CD**3** **704**. Fourth, two capture pulses of 66 MHz are applied to CK**4** **720** to detect or locate delay faults within the clock domain CD**4** **705**.

In addition, the delay faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1302** between the rising edge of the second capture pulse of CK**1** **711** and the rising edge of the first capture pulse of CK**2** **714** must be adjusted to meet the at-speed timing requirements for paths from **721** to **723**. Similarly, the relative clock delay **1304** between CK**2** **714** and CK**3** **717**, and the relative clock delay **1306** between CK**3** **717** and CK**4** **720**, must be adjusted to meet the at-speed timing requirements for paths from **725** to **727**, and paths from **729** and **731**, respectively.

FIG. **14** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating delay faults within each clock domain and stuck-at faults crossing clock domains with a reordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1400** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1408**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1409**, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of 66 MHz are applied to CK**4** **720** to detect or locate delay faults within the clock domain CD**4** **705**. Second, two capture pulses of 100 MHz are applied to CK**3** **717** to detect or locate delay faults within the clock domain CD**3** **704**. Third, two capture pulses of 100 MHz are applied to CK**2** **714** to detect or locate delay faults within the clock domain CD**2** **703**. Fourth, two capture pulses of 150 MHz are applied to CK**1** **711** to detect or locate delay faults within the clock domain CD**1** **702**.

In addition, the stuck-at faults which can be reached from lines **724**, **728**, and **732** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1402** between the rising edge of the second capture pulse of CK**4** **720** and the rising edge of the first capture pulse of CK**3** **717** must be adjusted so that no races or timing violations would occur while the output responses **730** are captured through the crossing clock-domain logic block CCD**3** **708**.

The same principle applies to the relative clock delay **1404** between CK**3** **717** and CK**2** **714**, and the relative clock delay **1406** between CK**2** **714** and CK**1** **711** for capturing output responses, **726** and **722**, through CCD**2** **707** and CCD**1** **706**, respectively.

FIG. **15** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating additional delay faults within each clock domain and additional stuck-at faults crossing clock domains with an expanded yet ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1500** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1514**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1515**, seven sets of double-capture pulses are applied in the following order: First, two capture pulses of 150 MHz are applied to CK**1** **711**. Second, two capture pulses of 100 MHz are applied to CK**2** **714**. Third, two capture pulses of 100 MHz are applied to CK**3** **717**. Fourth, two capture pulses of 66 MHz are applied to CK**4** **720**. Fifth, two capture pulses of 100 MHz are applied to CK**3** **717**. Sixth, two capture pulses of 100 MHz are applied to CK**2** **714**. Seventh, two capture pulses of 150 MHz are applied to CK**1** **711**.

For the capture clock CK**1** **711**, the second pulse and the third pulse are used to launch the transition needed for detecting or locating delay faults within the clock domain CD**1** **702**. Since the transition is generated by two close-to-functional patterns, the risk of activating a false path is lower. In addition, additional delay faults within the clock domain CD**1** **702** can be detected or located by the transition. The same results also apply to the clock domains CD**2** **703** and CD**3** **704**.

In addition, the stuck-at faults which can be reached from lines **724**, **728**, and **732** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1508** between the rising edge of the second capture pulse of CK**4** **720** and the rising edge of the first capture pulse of CK**3** **717** must be adjusted so that no races or timing violations would occur while the output responses **730** are captured through the crossing clock-domain logic block CCD**3** **708**.

The same principle applies to the relative clock delay **1510** between CK**3** **717** and CK**2** **714**, and the relative clock delay **1512** between CK**2** **714** and CK**1** **711** for capturing output responses, **726** and **722**, through CCD**2** **707** and CCD**1** **706**, respectively.

FIG. **16** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating 2-cycle delay faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that some paths in the clock domains, CD**1** **702** to CD**4** **705**, need two cycles for signals to pass through. The timing diagram **1600** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1608**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1609**, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of 75 MHz (half of 150 MHz) are applied to CK**1** **711** to detect or locate 2-cycle delay faults within the clock domain CD**1** **702**. Second, two capture pulses of 50 MHz (half of 100 MHz) are applied to CK**2** **714** to detect or locate 2-cycle delay faults within the clock domain CD**2** **703**. Third, two capture pulses of 50 MHz (half of 100 MHz) are applied to CK**3** **717** to detect or locate 2-cycle delay faults within the clock domain CD**3** **704**. Fourth, two capture pulses of 33 MHz (half of 66 MHz) are applied to CK**4** **720** to detect or locate 2-cycle delay faults within the clock domain CD**4** **705**.

In addition, the stuck-at faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1602** between the rising edge of the second capture pulse of CK**1** **711** and the rising edge of the first capture pulse of CK**2** **714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCD**1** **706**.

The same principle applies to the relative clock delay **1604** between CK**2** **714** and CK**3** **717**, and the relative clock delay **1606** between CK**3** **717** and CK**4** **720** for capturing output responses, **727** and **731**, through CCD**2** **707** and CCD**3** **708**, respectively.

FIG. **17** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating 2-cycle delay faults within each clock domain and 2-cycle delay faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that some paths in the clock domains, CD**1** **702** to CD**4** **705**, and the crossing clock-domain logic blocks, CCD**1** **706** to CCD**3** **708**, need two cycles for signals to pass through. The timing diagram **1700** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1708**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1709**, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of 75 MHz (half of 150 MHz) are applied to CK**1** **711** to detect or locate 2-cycle delay faults within the clock domain CD**1** **702**. Second, two capture pulses of 50 MHz (half of 100 MHz) are applied to CK**2** **714** to detect or locate 2-cycle delay faults within the clock domain CD**2** **703**. Third, two capture pulses of 50 MHz (half of 100 MHz) are applied to CK**3** **717** to detect or locate 2-cycle delay faults within the clock domain CD**3** **704**. Fourth, two capture

pulses of 33 MHz (half of 66 MHz) are applied to CK4 **720** to detect or locate 2-cycle delay faults within the clock domain CD4 **705**.

In addition, the 2-cycle delay faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD1 **706** to CCD3 **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1702** between the rising edge of the second capture pulse of CK1 **711** and the rising edge of the first capture pulse of CK2 **714** must be adjusted to meet the 2-cycle timing requirements for paths from **721** to **723**. Similarly, the relative clock delay **1704** between CK2 **714** and CK3 **717**, and the relative clock delay **1706** between CK3 **717** and CK4 **720**, must be adjusted to meet the 2-cycle timing requirements for paths from **725** to **727**, and paths from **729** and **731**, respectively.

FIG. **18** shows a timing diagram of a feed-forward partial-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that the clock domains CD1 **702** to CD4 **705** contain a number of un-scanned storage cells that form a sequential depth of no more than 2. The timing diagram **1800** shows the sequence of waveforms of the 4 capture clocks, CK1 **711** to CK4 **720**, operating at different frequencies.

During each shift cycle **1812**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK1 **711** to CK4 **720**, to shift stimuli to all scan cells within all clock domains, CD1 **702** to CD4 **705**.

During each capture cycle **1813**, 4 sets of capture clock pulses are applied in the following order: First, three pulses of 150 MHz, two being functional pulses and one being a capture pulse, are applied to CK1 **711** to detect or locate stuck-at faults within the clock domain CD1 **702**. Second, three pulses of 100 MHz, two being functional pulses and one being a capture pulse, are applied to CK2 **714** to detect or locate stuck-at faults within the clock domain CD2 **703**. Third, three pulses of 100 MHz, two being functional pulses and one being a capture pulse, are applied to CK3 **717** to detect or locate stuck-at faults within the clock domain CD3 **704**. Fourth, three pulses of frequency 66 MHz, two being functional pulses and one being a capture pulse, are applied to CK4 **717** to detect or locate stuck-at faults within the clock domain CD4 **705**.

In addition, the stuck-at faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD1 **706** to CCD3 **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1803** between the rising edge of the second capture pulse of CK1 **711** and the rising edge of the first capture pulse of CK2 **714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCD1 **706**.

The same principle applies to the relative clock delay **1806** between CK2 **714** and CK3 **717**, and the relative clock delay **1809** between CK3 **717** and CK4 **720** for capturing output responses, **727** and **731**, through CCD2 **707** and CCD3 **708**, respectively.

FIG. **19** shows a timing diagram of a feed-forward partial-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating delay faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that the clock domains CD1 **702** to CD4 **705** contain a number of un-scanned storage cells that form a sequential depth of no more than 2. The timing diagram **1900** shows the sequence of waveforms of the 4 capture clocks, CK1 **711** to CK4 **720**, operating at different frequencies.

During each shift cycle **1916**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK1 **711** to CK4 **720**, to shift stimuli to all scan cells within all clock domains, CD1 **702** to CD4 **705**.

During each capture cycle **1917**, 4 sets of capture clock pulses are applied in the following order: First, 4 pulses of 150MHZ, two being functional pulses and two being capture pulses, are applied to CK1 **711** to detect or locate delay faults within the clock domain CD1 **702**. Second, 4 pulses of 100 MHz, two being functional pulses and two being capture pulses, are applied to CK2 **714** to detect or locate delay faults within the clock domain CD2 **703**. Third, 4 pulses of 100 MHz, two being functional pulses and two being capture pulses, are applied to CK3 **717** to detect or locate delay faults within the clock domain CD3 **704**. Fourth, 4 pulses of 66 MHz, two being functional pulses and two being capture pulses, are applied to CK4 **720** to detect or locate delay faults within the clock domain CD4 **705**.

In addition, the stuck-at faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD1 **706** to CCD3 **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1904** between the rising edge of the second capture pulse of CK1 **711** and the rising edge of the first capture pulse of CK2 **714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCD1 **706**.

The same principle applies to the relative clock delay **1908** between CK2 **714** and CK3 **717**, and the relative clock delay **1912** between CK3 **717** and CK4 **720** for capturing output responses, **727** and **731**, through CCD2 **707** and CCD3 **708**, respectively.

FIG. **20** shows a timing diagram of a feed-forward partial-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating 2-cycle delay faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that the clock domains CD1 **702** to CD4 **705** contain a number of un-scanned storage cells that form a sequential depth of no more than 2. Also, it is assumed that some paths in the clock domains, CD1 **702** to CD4 **705**, need two cycles for signals to pass through. The timing diagram **2000** shows the sequence of waveforms of the 4 capture clocks, CK1 **711** to CK4 **720**, operating at different frequencies.

During each shift cycle **2016**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK1 **711** to CK4 **720**, to shift stimuli to all scan cells within all clock domains, CD1 **702** to CD4 **705**.

During each capture cycle **2017**, 4 sets of capture clock pulses are applied in the following order: First, 4 pulses, two being functional pulses of 150 MHz and two being capture pulses of 75 MHz (half of 150 MHz), are applied to CK1 **711** to detect or locate 2-cycle delay faults within the clock domain CD1 **702**. Second, 4 pulses, two being functional pulses of 100 MHz and two being capture pulses of 50 MHz

(half of 100 MHz), are applied to CK2 **714** to detect or locate 2-cycle delay faults within the clock domain CD2 **703**. Third, 4 pulses, two being functional pulses of 100 MHz and two being capture pulses of 50 MHz (half of 100 MHz), are applied to CK3 **717** to detect or locate 2-cycle delay faults within the clock domain CD3 **704**. Fourth, 4 pulses, 2 being functional pulses of 66 MHz and 2 being capture pulses of 33 MHz (half of 66 MHz), are applied to CK4 **720** to detect or locate 2-cycle delay faults within the clock domain CD4 **705**.

In addition, the stuck-at faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD1 **706** to CCD3 **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **2004** between the rising edge of the second capture pulse of CK1 **711** and the rising edge of the first capture pulse of CK2 **714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCD1 **706**.

The same principle applies to the relative clock delay **2008** between CK2 **714** and CK3 **717**, and the relative clock delay **2012** between CK3 **717** and CK4 **720** for capturing output responses, **727** and **731**, through CCD2 **707** and CCD3 **708**, respectively.

FIG. **21** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where the capture clock CK2 during the capture cycle is chosen to diagnose faults captured by CK2 in self-test or scan-test mode.

Fault diagnosis is the procedure by which a fault is located. In order to achieve this goal, it is often necessary to use an approach where a test pattern detects only portion of faults while guaranteeing no other faults are detected. If the test pattern does produce a response that matches the observed response, it can then be declared that the portion must contain at least one actual fault. Then the same approach to the portion of the faults to further localize the actual faults.

The timing diagram **2100** shows a way to facilitate this approach. In the capture cycle **2107**, two capture pulses of 100 MHz are only applied to the capture clock CK2 **714** while the other three capture clocks are held inactive. As a result, for delay faults, only those in the clock domain CD2 **703** are detected. In addition, for stuck-at faults, only those in the crossing clock-domain logic blocks CCD1 **706** and CCD2 **707** and the clock domain CD2 **703** are detected. Obviously, this clock timing helps in fault diagnosis.

FIG. **22** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where the capture clocks CK1 and CK3 during the capture cycle are chosen to diagnose faults captured by CK1 and CK3 in self-test or scan-test mode.

The diagram **2200** shows one more timing scheme that can help fault diagnosis as described in the description of FIG. **21**. In the capture cycle **2208**, two capture pulses of 150 MHz are applied to the capture clock CK1 **711** and two capture pulses of 100 MHz are applied to the capture clock CK3 **717** while the other two capture clocks are held inactive. As a result, for delay faults, only those in the clock domain CD1 **702** and CD3 **704** are detected. In addition, for stuck-at faults, only those in the crossing clock-domain logic blocks CCD1 **706** to CCD3 **708** and the clock domains CD1 **702** and CD3 **703** are detected. Obviously, this clock timing helps in fault diagnosis.

FIG. **23** shows a timing diagram of the full-scan design given in FIG. **1**, in accordance with the present invention, where all capture clocks during the shift cycle are skewed to reduce power consumption. The timing diagram **2300** only shows the waveforms for the capture clocks CK1 **111** to CK4 **120** during the shift cycle. For the capture cycle, any capture timing control methods claimed in this patent can be applied.

During the shift cycle **2305**, clock pulses for the clocks CK1 **111** to CK4 **120** are skewed by properly setting the delay **2301** between the shift pulses for the clocks CK1 **111** and CK2 **114**, the delay **2302** between the shift pulses for the clocks CK2 **114** and CK3 **117**, the delay **2303** between the shift pulses for the clocks CK3 **117** and CK4 **120**, the delay **2304** between the shift pulses for the clocks CK4 **120** and CK1 **111**. As a result, both peak power consumption and average power consumption are reduced. In addition, during the capture cycle, the PRPG **212** is driven by clock CK2 **114**, the first-arrived capture clock, and the MISR **221** is driven by clock CK3 **117**, the last-arrived capture clock, in the shared PRPG-MISR pair **228** in FIG. **2**. Thus, the ordered capture sequence guarantees the correct capture operation when a shared PRPG-MISR pair is used for a plurality of clock domains in self-test mode.

FIG. **24** shows a flow chart of one embodiment of the invention. The multiple-capture self-test computer-aided design (CAD) system **2400** accepts the user-supplied HDL code or netlist **2402** together with the self-test control files **2401** and the chosen foundry library **2403**. The self-test control files **2401** contain all set-up information and scripts required for compilation **2404**, self-test rule check **2406**, self-test rule repair **2507**, and multiple-capture self-test synthesis **2408**. As a result, an equivalent combinational circuit model **2409** is generated. Then, combinational fault simulation **2410** can be performed. Finally, post-processing **2411** is used to produce the final self-test HDL code or netlist **2412** as well as the HDL test benches and ATE test programs **2413**. All reports and errors are saved in the report files **2414**.

The multiple-capture self-test synthesis **2408** uses a hierarchical approach in which it synthesizes a plurality of PRPG-MISR pairs one at a time for each individual clock domain or combined clock domains, then synthesizes a central self-test controller which includes an error indicator, and finally stitches the central self-test controller together with synthesized PRPG-MISR pairs. Each PRPG-MISR pair is composed of a PRPG, an optional phase shifter, an optional space compactor, a MISR, and a comparator. In addition, during PRPG-MISR synthesis, a number of spare scan cells can be inserted into selected clock domains. As a result, the central self-test controller can remain intact even when the need for circuit modification rises at a later stage.

FIG. **25** shows a flow chart of one embodiment of the invention. The multiple-capture scan-test computer-aided design (CAD) system **2500** accepts the user-supplied HDL code or netlist **2502** together with the scan control files **2501** and the chosen foundry library **2503**. The scan control files **2501** contain all set-up information and scripts required for compilation **2504**, scan rule check **2506**, scan rule repair **2507**, and multiple-capture scan synthesis **2508**. As a result, an equivalent combinational circuit model **2509** is generated. Then, combinational ATPG **2510** can be performed. Finally, post-processing **2511** is used to produce the final scan HDL netlist **2512** as well as the HDL test benches and ATE test programs **2513**. All reports and errors are saved in the report files **2514**.

Having thus described presently preferred embodiments of the present invention, it can now be appreciated that the objectives of the invention have been fully achieved. And it

will be understood by those skilled in the art that many changes in construction & circuitry, and widely differing embodiments & applications of the invention will suggest themselves without departing from the spirit and scope of the present invention. The disclosures and the description herein are intended to be illustrative and are not in any sense limitation of the invention, more preferably defined in the scope of the invention by the Claims appended hereto and their equivalents.

What is claimed is:

1. A method for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly during self-test, where N>1, each clock domain having one or more capture clocks and one or more scan cells, each capture clock comprising a selected number of shift clock pulses and a selected number of capture clock pulses, each shift clock pulse comprising a clock pulse applied in scan mode, each capture clock pulse comprising a clock pulse applied in normal mode; said method comprising the steps of:

(a) generating and loading N pseudorandum stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly, by applying said shift clock pulses to all said scan cells in said scan mode for loading or shifting-in said N pseudorandom stimuli to all said scan cells, during a shift operation;

(b) applying an ordered sequence of capture clock pulses to all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture clock pulses comprising at least two capture clock pulses from two or more selected capture clocks, for controlling two or more clock domains, in a sequential order, wherein each said selected capture clock must contain at least one said capture clock pulse, and when detecting or locating selected delay faults within a clock domain, said selected capture clock controlling the clock domain contains at least two consecutive said capture clock pulses to launch the transition and capture the output response; and

(c) compacting N output responses of all said scan cells to signatures, by applying said shift clock pulses to all said scan cells in said scan mode for compacting or shifting-out said N output responses to form said signatures, during a compact operation.

2. The method of claim **1**, wherein each said capture clock is programmable to contain said selected number of shift clock pulses and said selected number of capture clock pulses for performing said shift/compact and capture operation on all said scan cells within a selected clock domain controlled by said capture clock; wherein all said shift clock pulses and said capture clock pulses in said capture clock are selectively generated internally or controlled externally, and can be selectively operated at their rated clock speed (at-speed) or at a selected clock speed.

3. The method of claim **1**, further comprising providing N scan enable (SE) signals each controlling a selected clock domain; wherein all said scan enable (SE) signals are used to switch operations from shift/compact to capture, and vice versa; and wherein each said scan enable (SE) signal is selectively generated internally or controlled externally, and can be selectively operated at its rated clock speed or at a selected clock speed.

4. The method of claim **3**, wherein said providing N scan enable (SE) signals further comprises using one global scan enable (GSE) signal to drive all said scan enable (SE) signals so that said global scan enable (GSE) signal and all said scan enable (SE) signals can be operated at a selected reduced clock speed.

5. The method of claim **1**, wherein said generating and loading N pseudorandom stimuli further comprises operating all said shift clock pulses at selected clock speeds or at the same clock speed; wherein all said shift clock pulses are selectively skewed so that at any given time only one or more said scan cells are changing states to reduce power consumption.

6. The method of claim **1**, further comprising the step of comparing said signatures with their expected signatures for error indication, after a predetermined limiting criterion is reached; wherein said step of comparing said signatures with their expected signatures further comprises comparing said signatures inside said integrated circuit or circuit assembly or shifting-out said signatures for comparison in an ATE (automatic test equipment).

7. The method of claim **1**, wherein said generating and loading N pseudorandom stimuli further comprises using one or more pseudorandom pattern generators (PRPGs) to generate said N pseudorandom stimuli.

8. The method of claim **7**, wherein said pseudorandom pattern generator (PRPG) further comprises using a phase shifter connected to said PRPG outputs to generate one or more said pseudorandom stimuli.

9. The method of claim **8**, wherein said phase shifter is a linear logic network comprising one or more Exclusive-OR (XOR) or Exclusive-NOR (XNOR) gates.

10. The method of claim **1**, wherein said applying an ordered sequence of capture clock pulses further comprises applying said capture clock pulses concurrently to two or more selected clock domains which do not interact with each other or do not have any logic block crossing each other, for detecting or locating said faults in said selected clock domains.

11. The method of claim **1**, wherein said applying an ordered sequence of capture clock pulses further comprises applying a reversed ordered sequence of capture clock pulses from said ordered sequence of capture clock pulses, for detecting or locating additional faults in said integrated circuit or circuit assembly.

12. The method of claim **1**, wherein said applying an ordered sequence of capture clock pulses further comprises selectively applying a shortened or expanded ordered sequence of capture clock pulses from said ordered sequence of capture clock pulses, for detecting or locating additional faults in said integrated circuit or circuit assembly.

13. The method of claim **1**, wherein said applying an ordered sequence of capture clock pulses further comprises disabling all capture clock pulses in one or more capture clocks, to facilitate fault diagnosis.

14. The method of claim **1**, wherein said applying an ordered sequence of capture clock pulses further comprises selectively operating all said capture clock pulses controlling a selected clock domain at a selected clock speed, for detecting or locating stuck-at faults within said selected clock domain.

15. The method of claim **1**, wherein said applying an ordered sequence of capture clock pulses further comprises selectively operating all said capture clock pulses controlling a selected clock domain at their rated clock speed, for detecting or locating delay faults within said selected clock domain.

16. The method of claim **1**, wherein said applying an ordered sequence of capture clock pulses further comprises selectively reducing the speed of all said capture clock

pulses controlling a selected clock domain to the level where delay faults associated with all multiple-cycle paths of equal cycle latency within said selected clock domain are detected or located at a predetermined rated clock speed.

17. The method of claim **1**, wherein said applying an ordered sequence of capture clock pulses further comprises selectively operating all said capture clock pulses controlling two selected clock domains at selected clock speeds, for detecting or locating stuck-at faults crossing said two selected clock domains.

18. The method of claim **1**, wherein said applying an ordered sequence of capture clock pulses further comprises selectively adjusting the relative clock delay of two said capture clock pulses controlling two selected clock domains, for detecting or locating delay faults crossing said two selected clock domains.

19. The method of claim **1**, wherein said applying an ordered sequence of capture clock pulses further comprises selectively adjusting the relative clock delay of two said capture clock pulses controlling two selected clock domains to the level, where delay faults associated with all multiple-cycle paths of equal cycle latency crossing said two selected clock domains are detected or located at a predetermined rated clock speed.

20. The method of claim **1**, wherein said applying an ordered sequence of capture clock pulses further comprises controlling the relative clock delay between any two adjacent capture clock pulses inside or external to said integrated circuit or circuit assembly.

21. The method of claim **1**, wherein said compacting N output responses further comprises using one or more multiple-input signature registers (MISRs) to generate said signatures.

22. The method of claim **21**, wherein said multiple-input signature register (MISR) further comprises using a space compactor connected to said MISR inputs for compressing said output responses to generate one or more said signatures.

23. The method of claim **22**, wherein said space compactor is a linear logic network comprising one or more Exclusive-OR (XOR) or Exclusive-NOR (XNOR) gates.

24. The method of claim **1**, further comprising using a PRPG-MISR (pseudorandom pattern generator and multiple-input signature register) pair to detect or locate said faults within one or more selected clock domains when all said capture clocks controlling said selected clock domains operate at the same clock speed; wherein all said capture clocks are selectively skewed so as to eliminate races and timing violation during said shift, said capture, or said compact operation.

25. The method of claim **24**, wherein said PRPG-MISR pair further comprises a PRPG, selectively a phase shifter, selectively a space compactor, a MISR, and selectively a comparator.

26. The method of claim **1**, wherein said compacting N output responses further comprises selectively comparing said N output responses directly with their expected output responses and indicating errors immediately using a compare operation.

27. The method of claim **1**, wherein said scan cell is selectively a multiplexed D flip-flop or a level-sensitive scan latch, and further wherein said integrated circuit or circuit assembly under test is a full-scan or partial-scan design.

28. The method of claim **1**, wherein said faults further comprise stuck-at faults and delay faults; wherein said stuck-at faults further comprise other stuck-type faults, such as open faults and bridging faults, and wherein said delay faults further comprise other non-stuck-type delay faults, such as transition (gate-delay) faults, multiple-cycle delay faults, and path-delay faults.

29. An apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly during self-test, where N>1, each clock domain having one or more capture clocks and one or more scan cells, each capture clock comprising a selected number of shift clock pulses and a selected number of capture clock pulses, each shift clock pulse comprising a clock pulse applied in scan mode, each capture clock pulse comprising a clock pulse applied in normal mode; said apparatus comprising:

(a) means for generating and loading N pseudorandom stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly, by applying said shift clock pulses to all said scan cells in said scan mode for loading or shifting-in said N pseudorandom stimuli to all said scan cells, during a shift operation;

(b) means for applying an ordered sequence of capture clock pulses to all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture clock pulses comprising at least two said capture clock pulses from two or more selected capture clocks for controlling two or more clock domains, in a sequential order, wherein each said selected capture clock must contain at least one said capture clock pulse, and when detecting or locating selected delay faults within a clock domain, said selected capture clock controlling the clock domain contains at least two consecutive said capture clock pulses to launch the transition and capture the output response; and

(c) means for compacting N output responses of all said scan cells to signatures, by applying said shift clock pulses to all said scan cells in said scan mode for compacting or shifting-out said N output responses to form said signatures, during a compact operation.

30. The apparatus of claim **29**, wherein each said means of (a)–(c) is selectively placed inside or external to said integrated circuit or circuit assembly.

* * * * *

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Wang et al.

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(45) **Date of Patent: Oct. 7, 2008**

(54) **COMPUTER-AIDED DESIGN (CAD) MULTIPLE-CAPTURE DFT SYSTEM FOR DETECTING OR LOCATING CROSSING CLOCK-DOMAIN FAULTS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(62) Division of application No. 11/098,703, filed on Apr. 5, 2005, now Pat. No. 7,260,756, which is a division of application No. 10/067,372, filed on Feb. 7, 2002, now Pat. No. 7,007,213.

(60) Provisional application No. 60/268,601, filed on Feb. 15, 2001.

(51) **Int. Cl.**
G01R 31/28 (2006.01)
G06F 17/50 (2006.01)

(52) **U.S. Cl.** **714/724**; 703/14

(58) **Field of Classification Search** .... None
See application file for complete search history.

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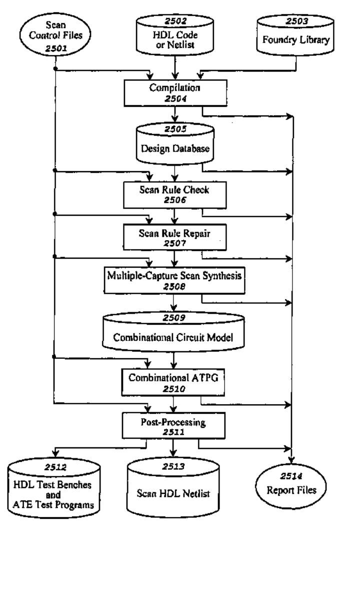
(57) **ABSTRACT**

A method and apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in self-test or scan-test mode, where N>1 and each domain has a plurality of scan cells. The method and apparatus allows generating and loading N pseudorandom or predetermined stimuli to all the scan cells within the N clock domains in the integrated circuit or circuit assembly during the shift operation, applying an ordered sequence of capture clocks to all the scan cells within the N clock domains during the capture operation, compacting or comparing N output responses of all the scan cells for analysis during the compact/compare operation, and repeating the above process until a predetermined limiting criteria is reached. A computer-aided design (CAD) system is further developed to realize the method and synthesize the apparatus.

7 Claims, 25 Drawing Sheets



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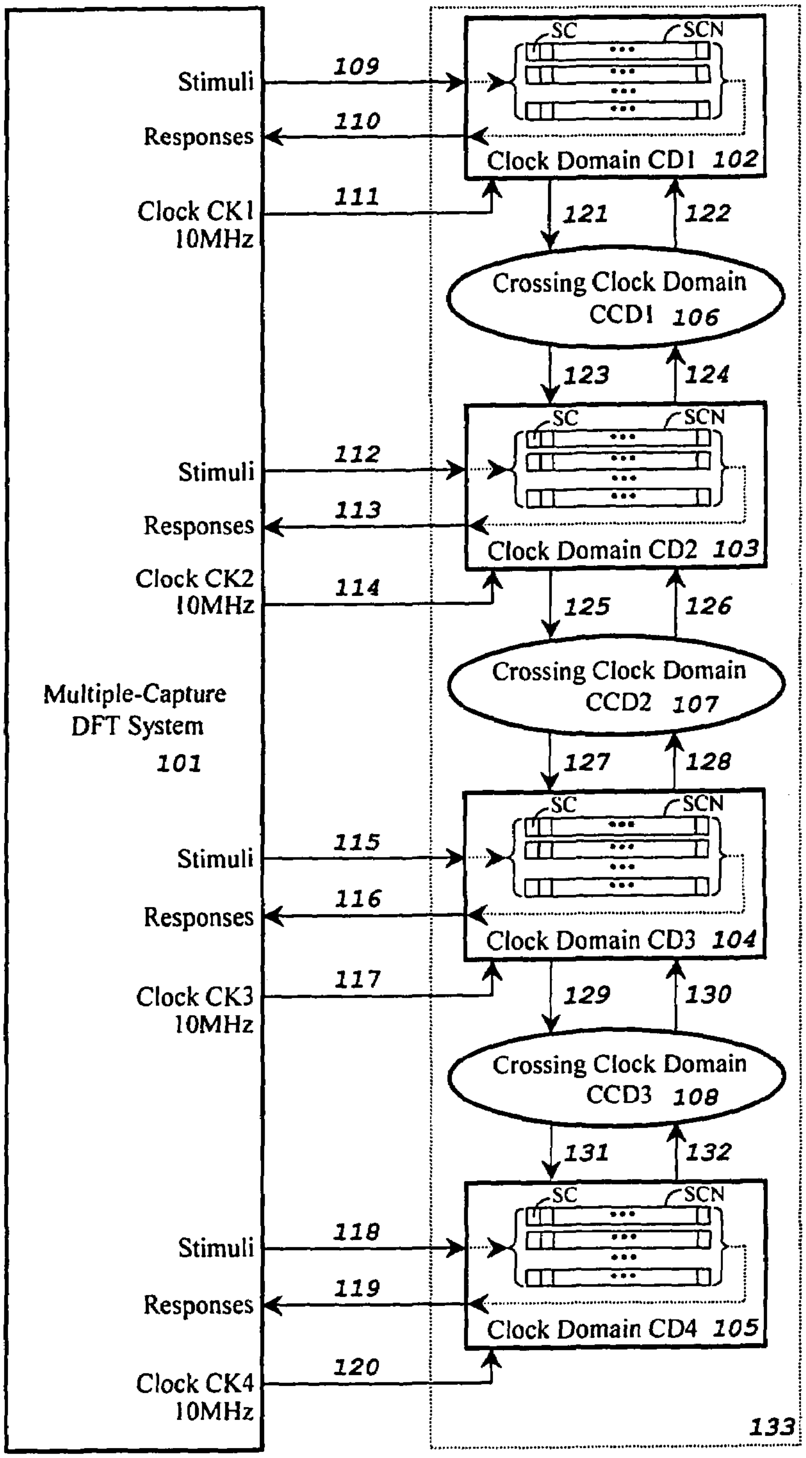
Stimuli
109
Responses
110
Clock CK1
10MHz
111
SC
SCN
Clock Domain CD1 102
121
122
Crossing Clock Domain
CCD1 106
123
124
Stimuli
112
Responses
113
Clock CK2
10MHz
114
Clock Domain CD2 103
125
126
Crossing Clock Domain
CCD2 107
127
128
Multiple-Capture
DFT System
101
Stimuli
115
Responses
116
Clock CK3
10MHz
117
Clock Domain CD3 104
129
130
Crossing Clock Domain
CCD3 108
131
132
Stimuli
118
Responses
119
Clock CK4
10MHz
120
Clock Domain CD4 105
133

FIG. 1

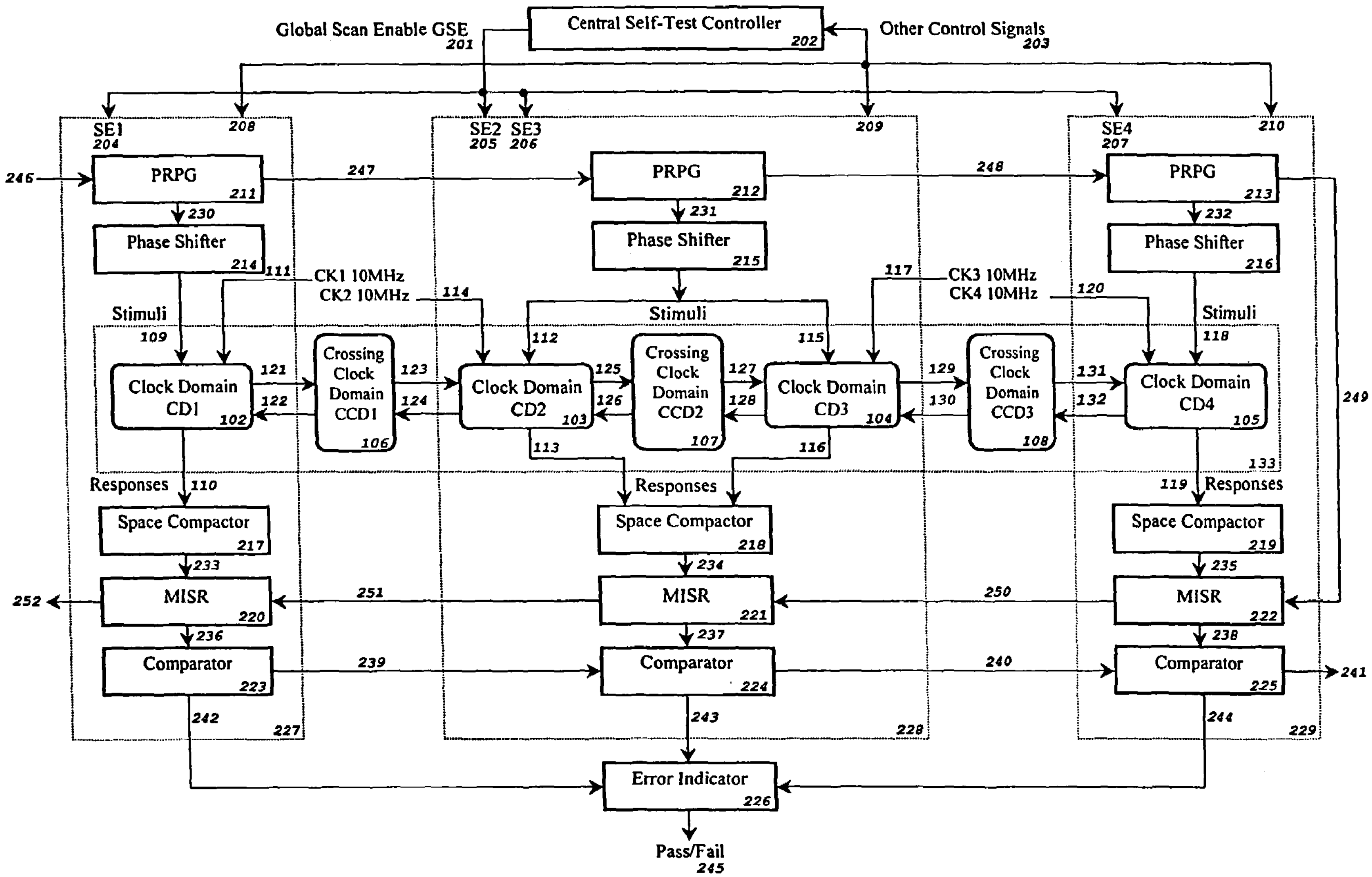
Central Self-Test Controller
202
Global Scan Enable GSE
201
Other Control Signals
203
SE1
204
208
SE2
205
SE3
206
209
SE4
207
210
246
PRPG
211
247
PRPG
212
248
PRPG
213
230
231
232
Phase Shifter
214
Phase Shifter
215
Phase Shifter
216
111
CK1 10MHz
CK2 10MHz
114
117
CK3 10MHz
CK4 10MHz
120
Stimuli
109
Stimuli
112
115
Stimuli
118
Clock Domain
CD1
102
121
122
Crossing
Clock
Domain
CCD1
106
123
124
Clock Domain
CD2
103
125
126
Crossing
Clock
Domain
CCD2
107
127
128
Clock Domain
CD3
104
129
130
Crossing
Clock
Domain
CCD3
108
131
132
Clock Domain
CD4
105
249
113
116
133
Responses
110
Responses
119
Responses
Space Compactor
217
Space Compactor
218
Space Compactor
219
233
234
235
252
MISR
220
251
MISR
221
250
MISR
222
236
237
238
Comparator
223
239
Comparator
224
240
Comparator
225
241
242
227
243
228
244
229
Error Indicator
226
Pass/Fail
245

FIG. 2

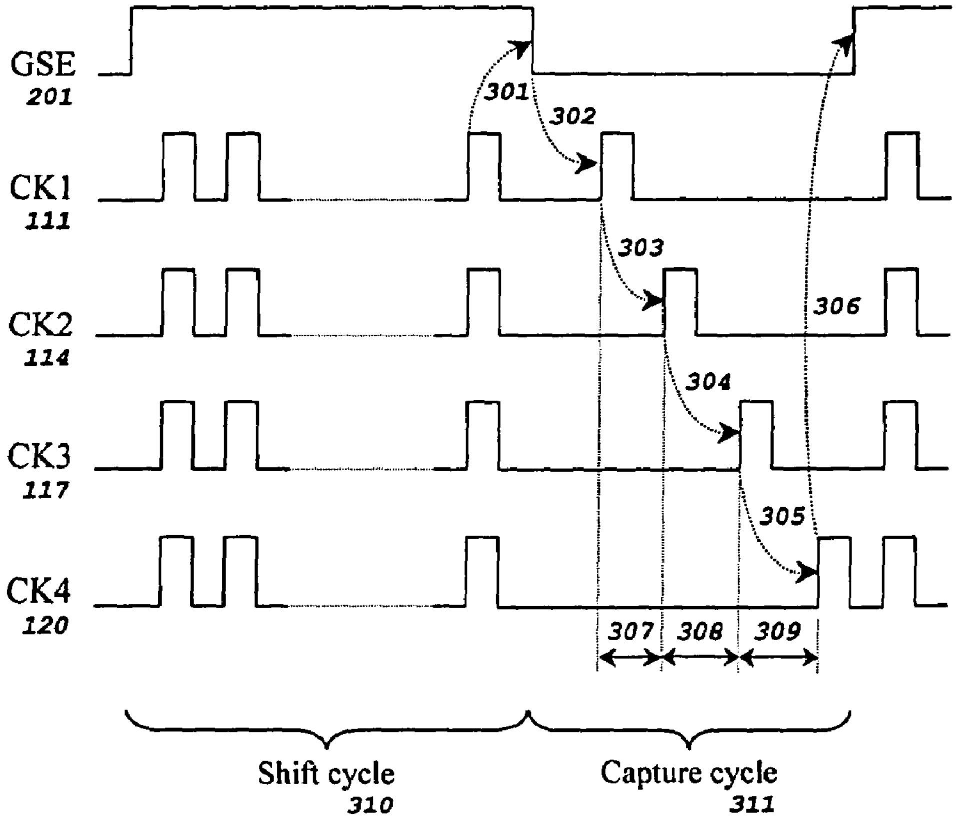
GSE
201
CK1
111
CK2
114
CK3
117
CK4
120
301
302
303
304
305
306
307
308
309
Shift cycle
310
Capture cycle
311

FIG. 3

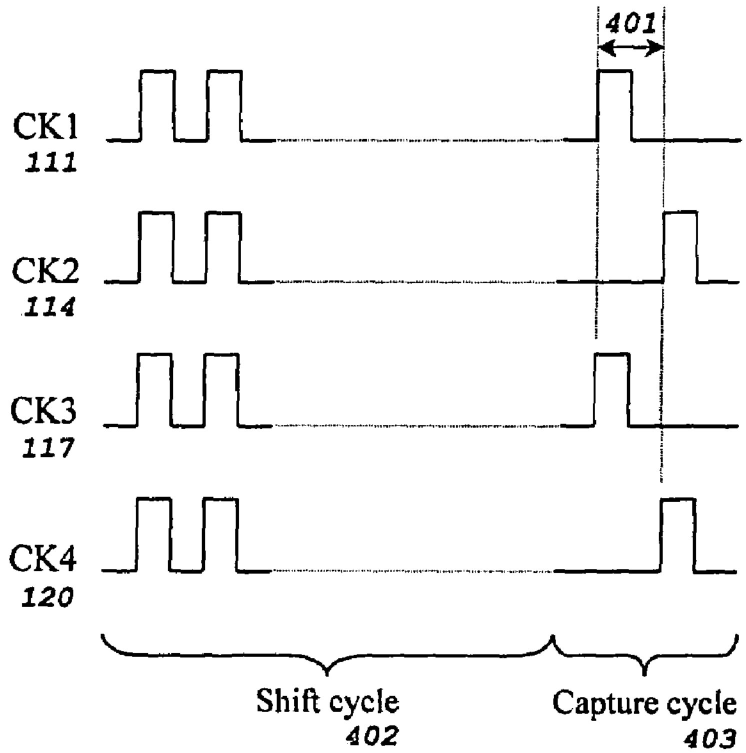
401
CK1
111
CK2
114
CK3
117
CK4
120
Shift cycle
402
Capture cycle
403

FIG. 4

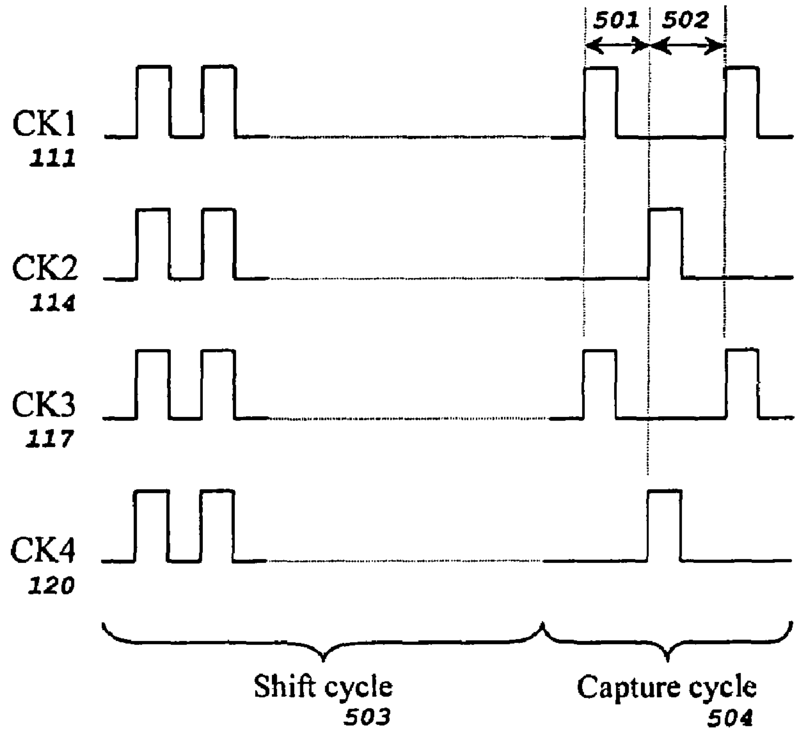
501
502
CK1
111
CK2
114
CK3
117
CK4
120
Shift cycle
503
Capture cycle
504

FIG. 5

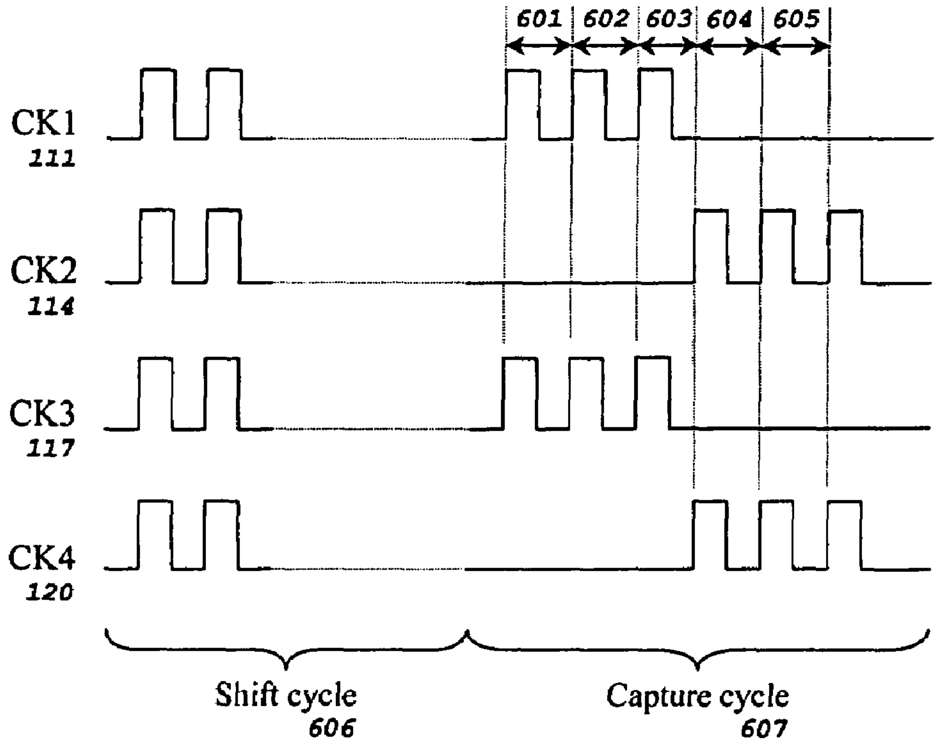
601
602
603
604
605
CK1
111
CK2
114
CK3
117
CK4
120
Shift cycle
606
Capture cycle
607

FIG. 6

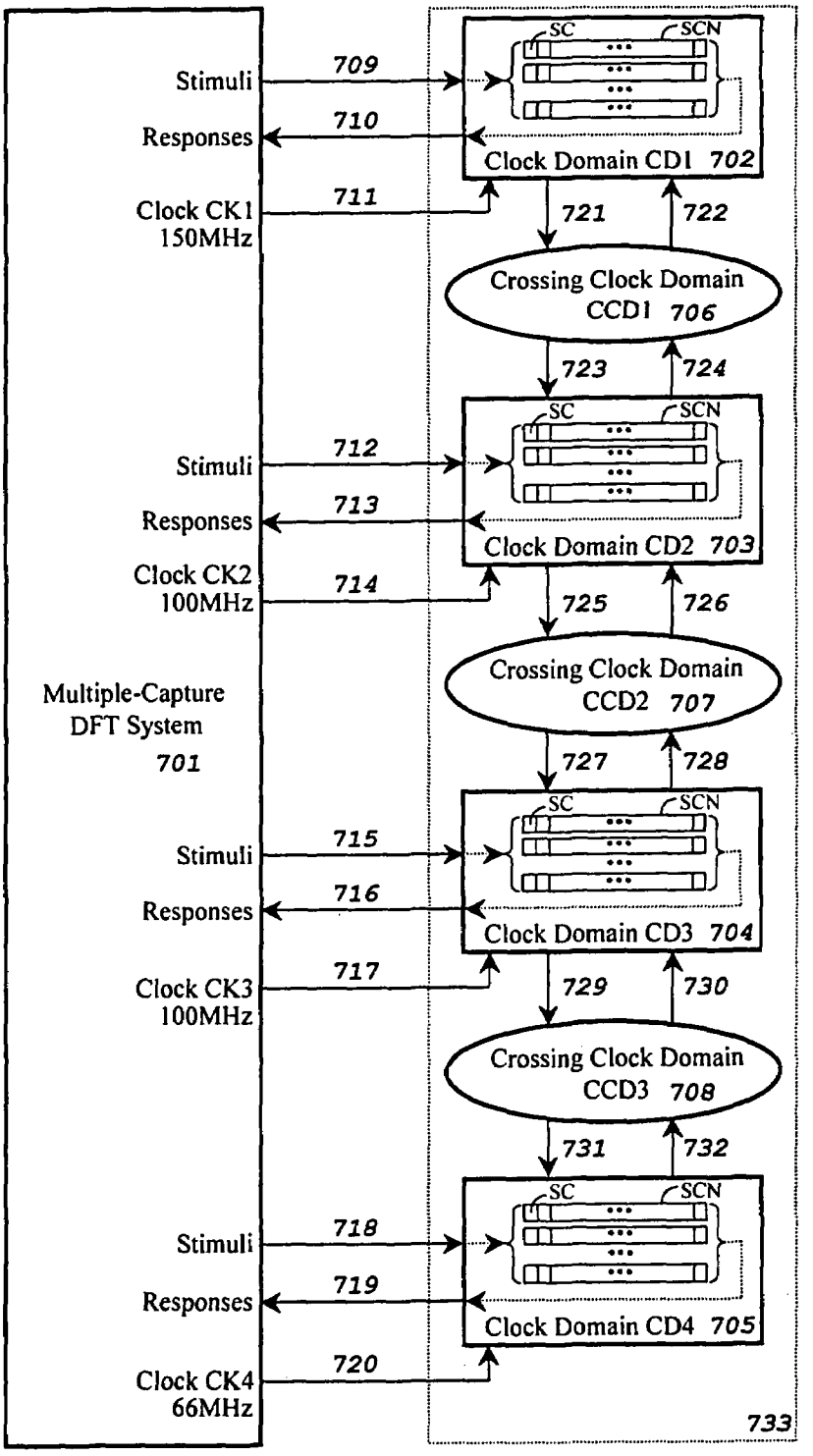
Stimuli
Responses
Clock CK1
150MHz
Clock CK2
100MHz
Clock CK3
100MHz
Clock CK4
66MHz
Multiple-Capture
DFT System
701
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
SC
SCN
Clock Domain CD1 702
Clock Domain CD2 703
Clock Domain CD3 704
Clock Domain CD4 705
Crossing Clock Domain
CCD1 706
Crossing Clock Domain
CCD2 707
Crossing Clock Domain
CCD3 708
733

FIG. 7

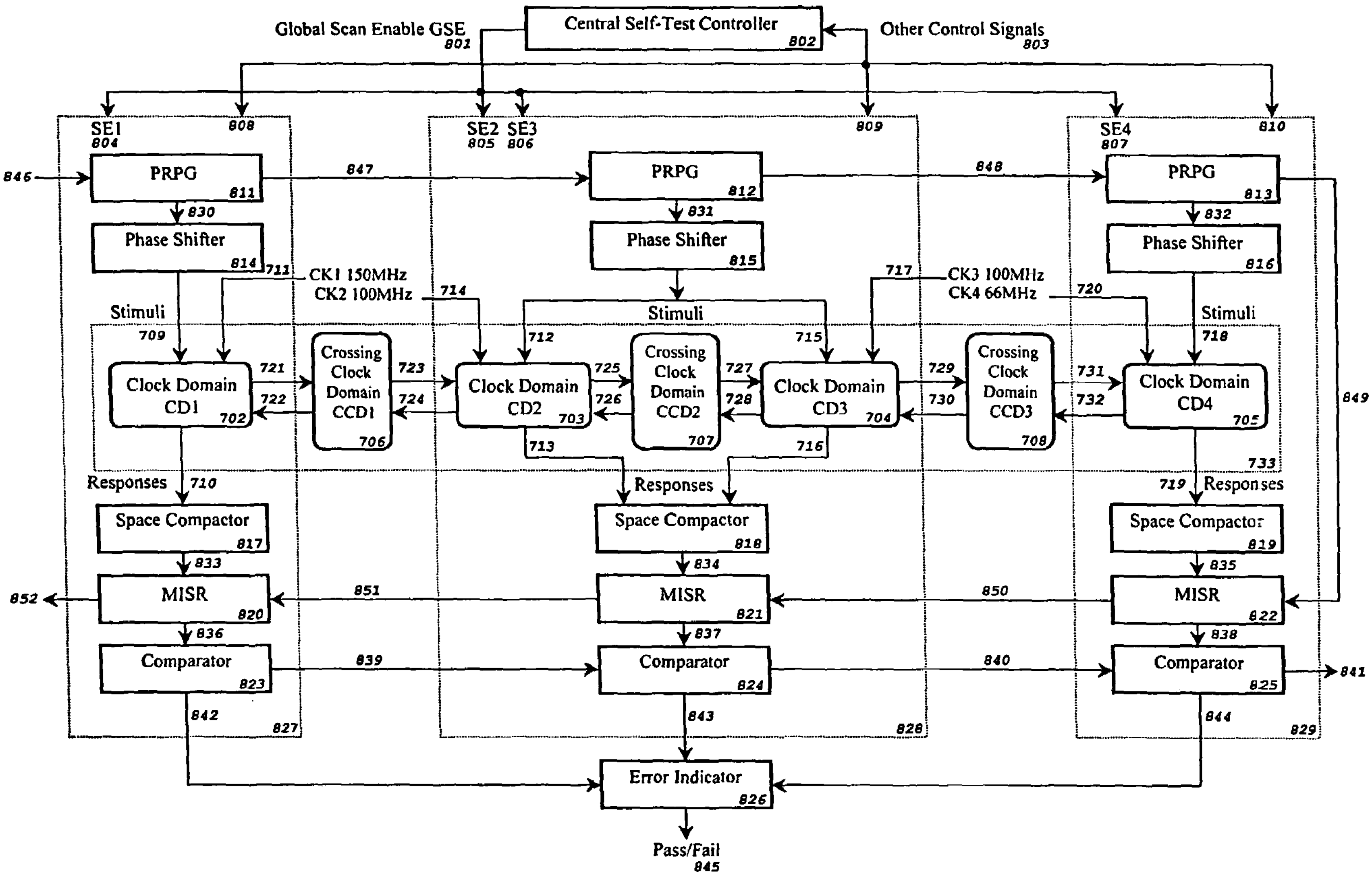
Central Self-Test Controller
802
Global Scan Enable GSE
801
Other Control Signals
803
SE1
804
808
SE2 SE3
805 806
809
SE4
807
810
846
PRPG
811
847
PRPG
812
848
PRPG
813
830
831
832
Phase Shifter
814
Phase Shifter
815
Phase Shifter
816
711
CK1 150MHz
CK2 100MHz
714
717
CK3 100MHz
CK4 66MHz
720
Stimuli
709
Stimuli
712
715
Stimuli
718
Clock Domain
CD1
702
721
722
Crossing
Clock
Domain
CCD1
706
723
724
Clock Domain
CD2
703
725
726
Crossing
Clock
Domain
CCD2
707
727
728
Clock Domain
CD3
704
729
730
Crossing
Clock
Domain
CCD3
708
731
732
Clock Domain
CD4
705
733
849
713
716
Responses
710
Responses
719
Responses
Space Compactor
817
Space Compactor
818
Space Compactor
819
833
834
835
MISR
820
851
MISR
821
850
MISR
822
852
836
837
838
Comparator
823
839
Comparator
824
840
Comparator
825
841
842
843
844
827
828
829
Error Indicator
826
Pass/Fail
845

FIG. 8

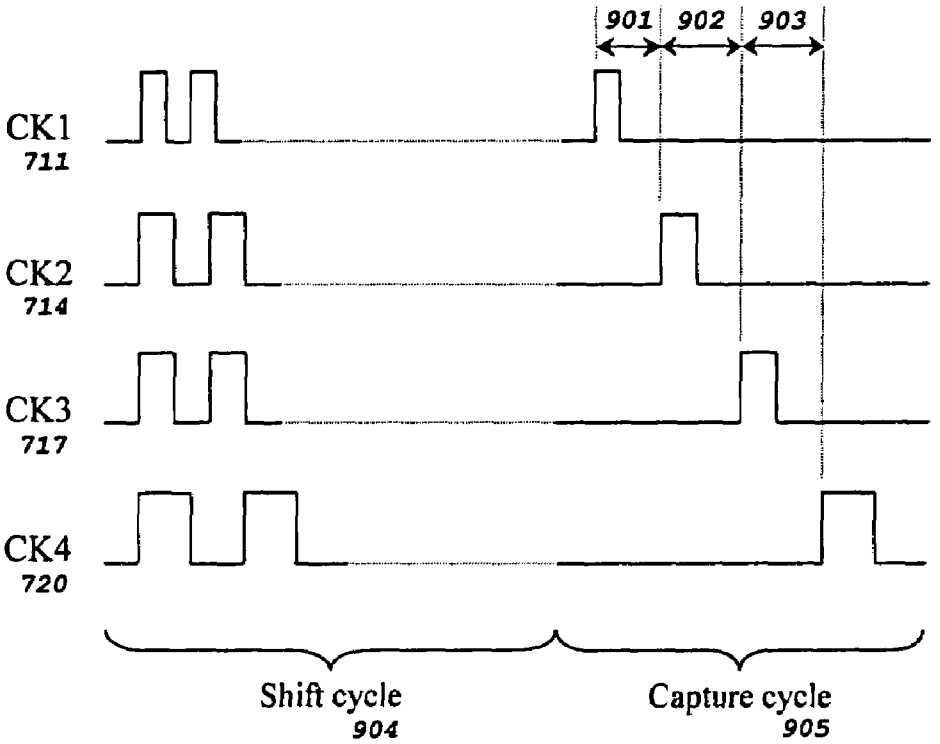
901
902
903
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
904
Capture cycle
905

FIG. 9

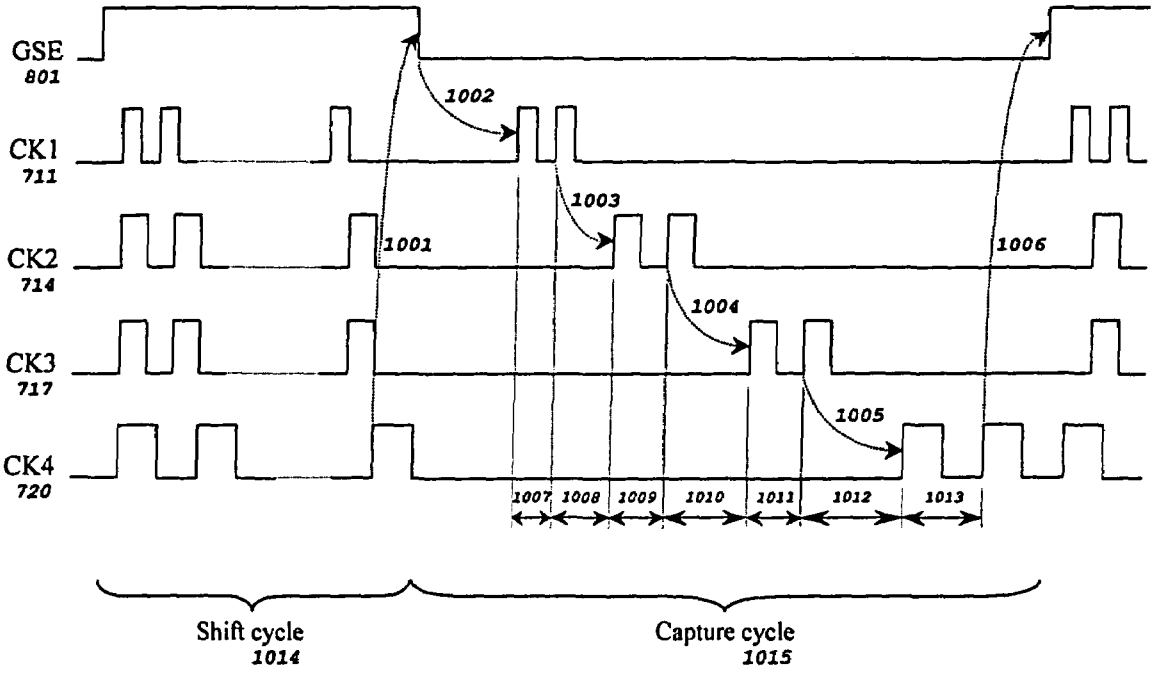
GSE
801
CK1
711
CK2
714
CK3
717
CK4
720
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
Shift cycle
1014
Capture cycle
1015

FIG. 10

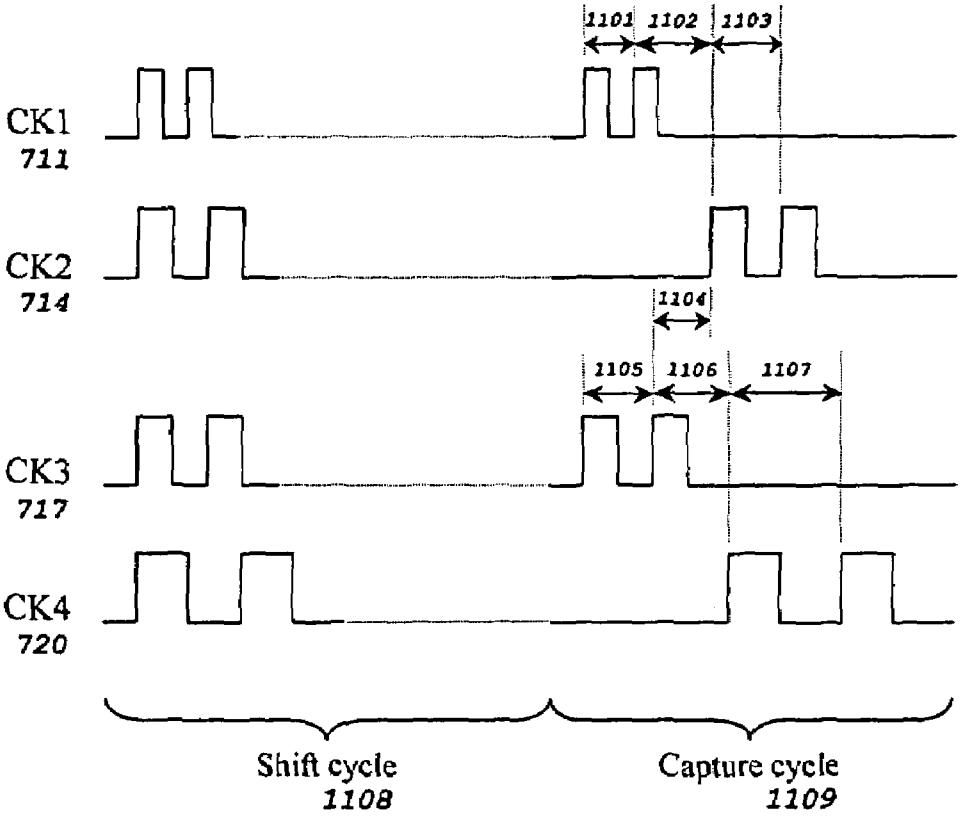
1101
1102
1103
CK1
711
CK2
714
1104
1105
1106
1107
CK3
717
CK4
720
Shift cycle
1108
Capture cycle
1109

FIG. 11

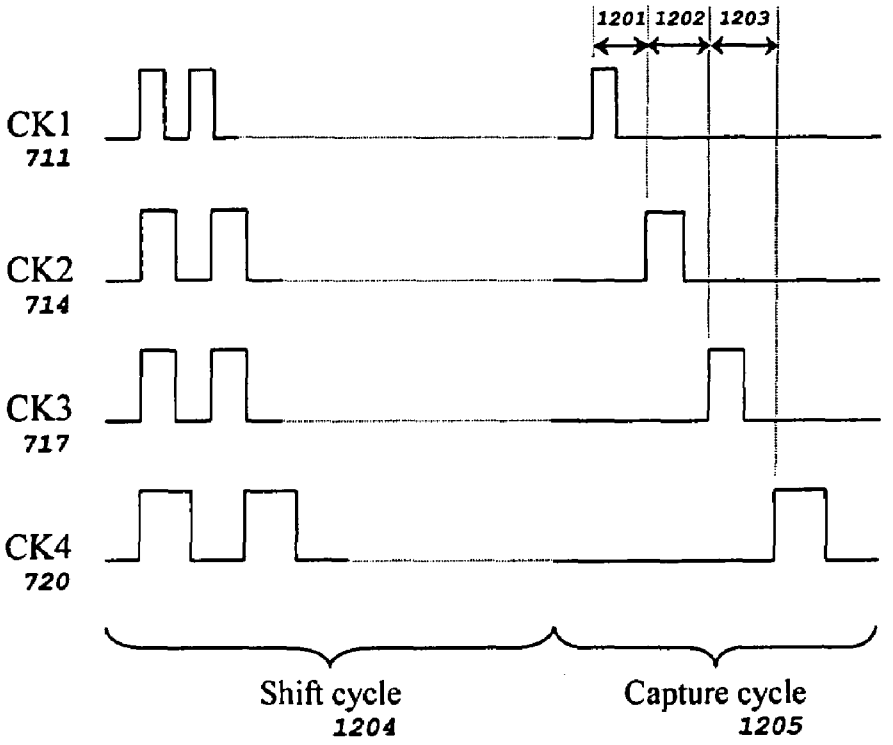
1201
1202
1203
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1204
Capture cycle
1205

FIG. 12

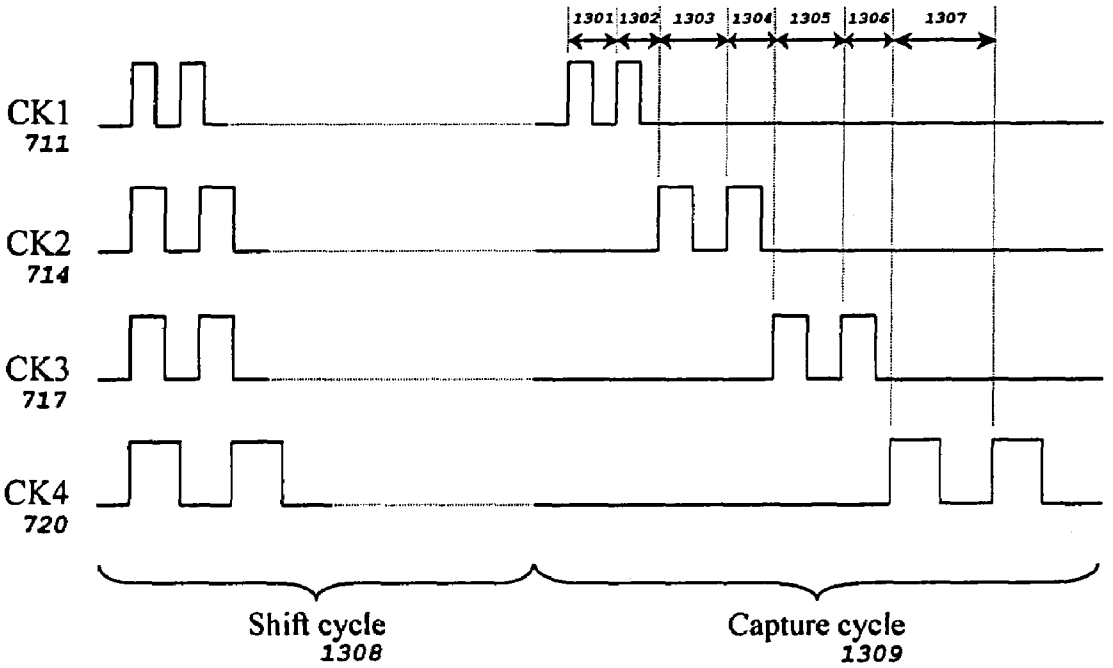
1301
1302
1303
1304
1305
1306
1307
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1308
Capture cycle
1309

FIG. 13

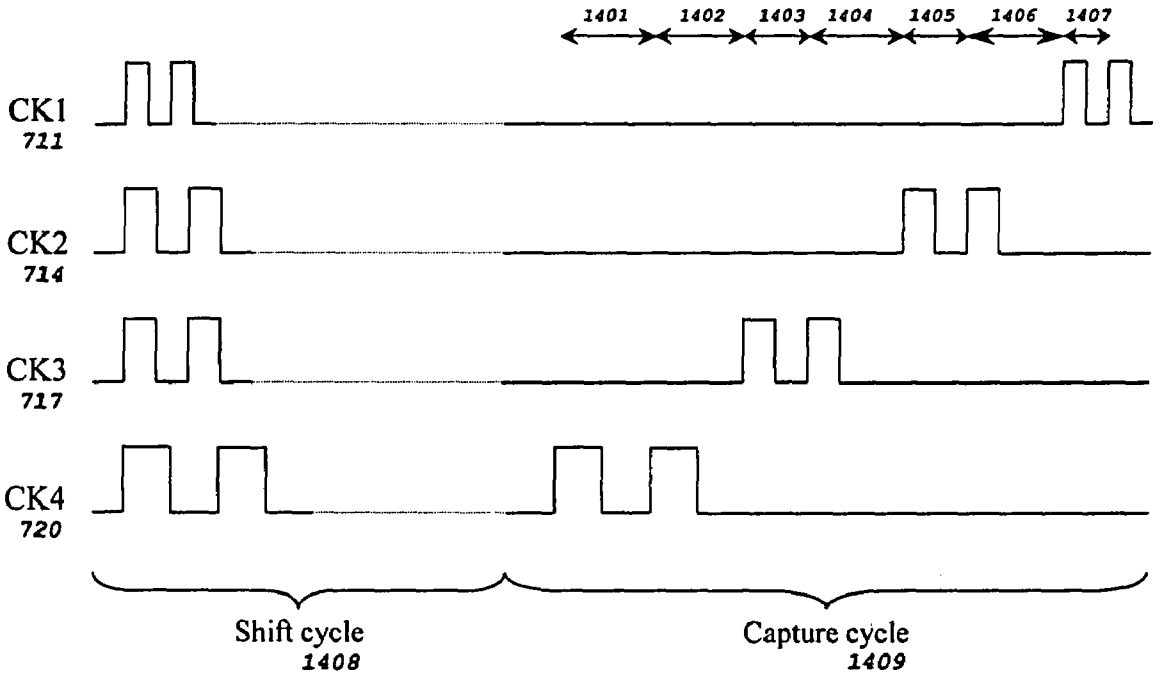
1401
1402
1403
1404
1405
1406
1407
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1408
Capture cycle
1409

FIG. 14

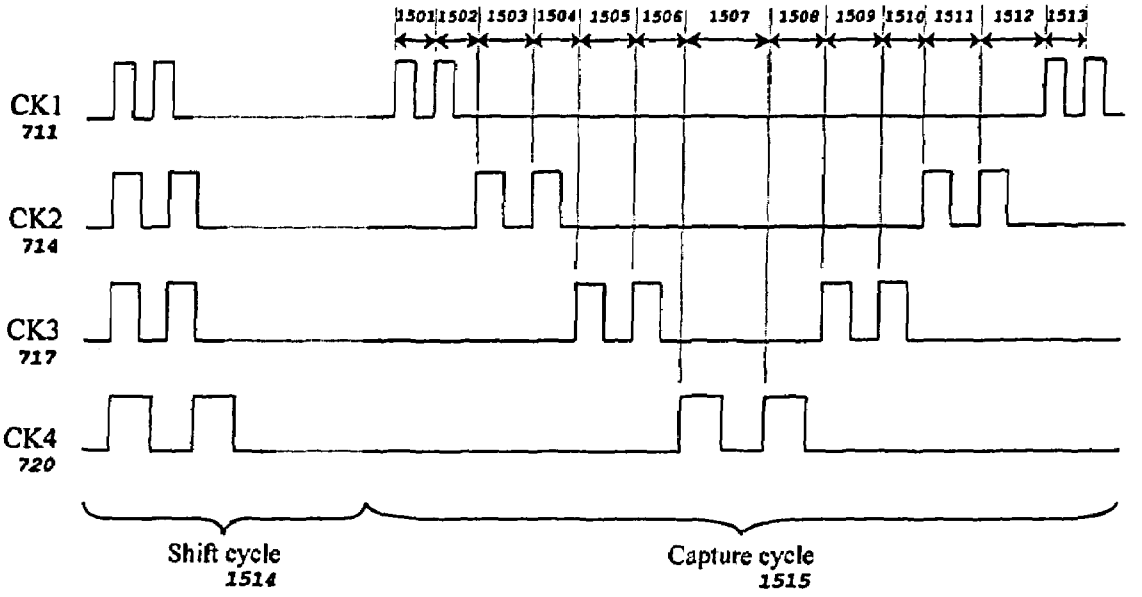
1501 1502 1503 1504 1505 1506 1507 1508 1509 1510 1511 1512 1513
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1514
Capture cycle
1515

FIG. 15

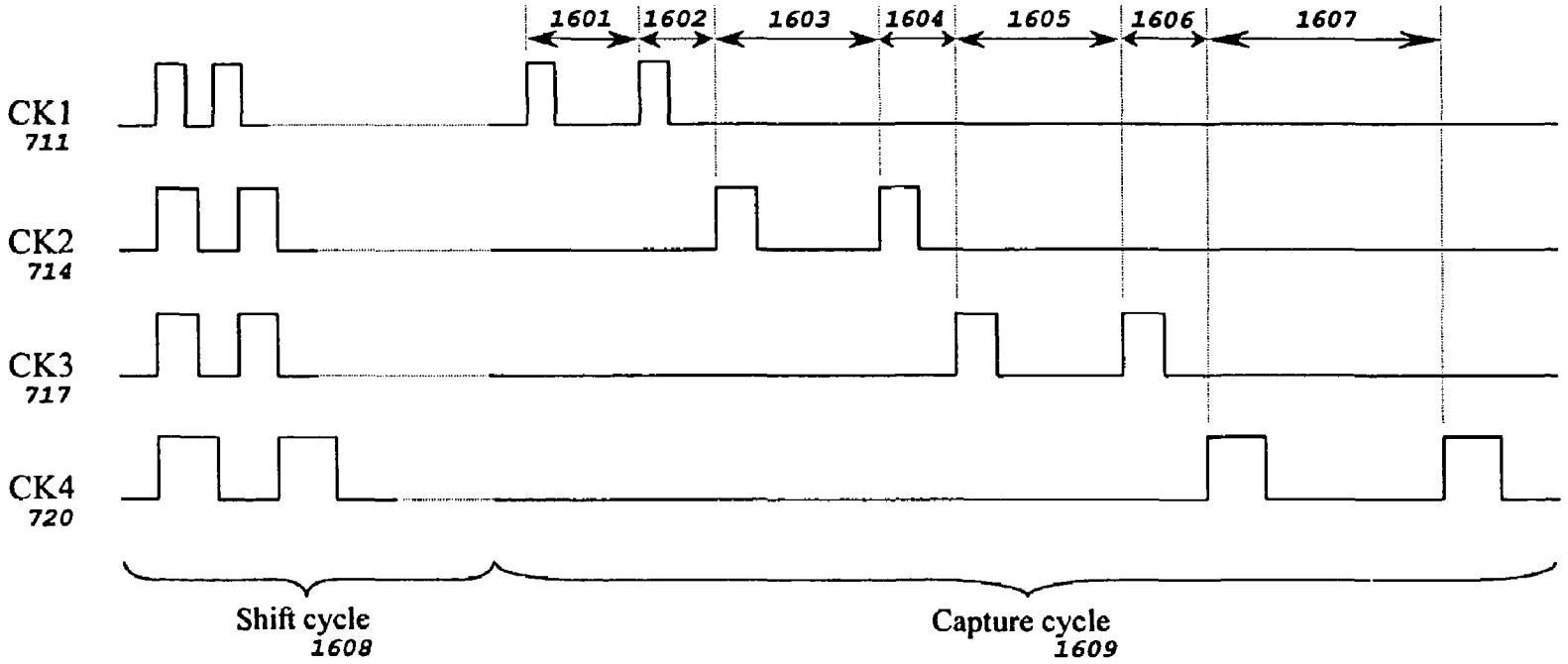
1601
1602
1603
1604
1605
1606
1607
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1608
Capture cycle
1609

FIG. 16

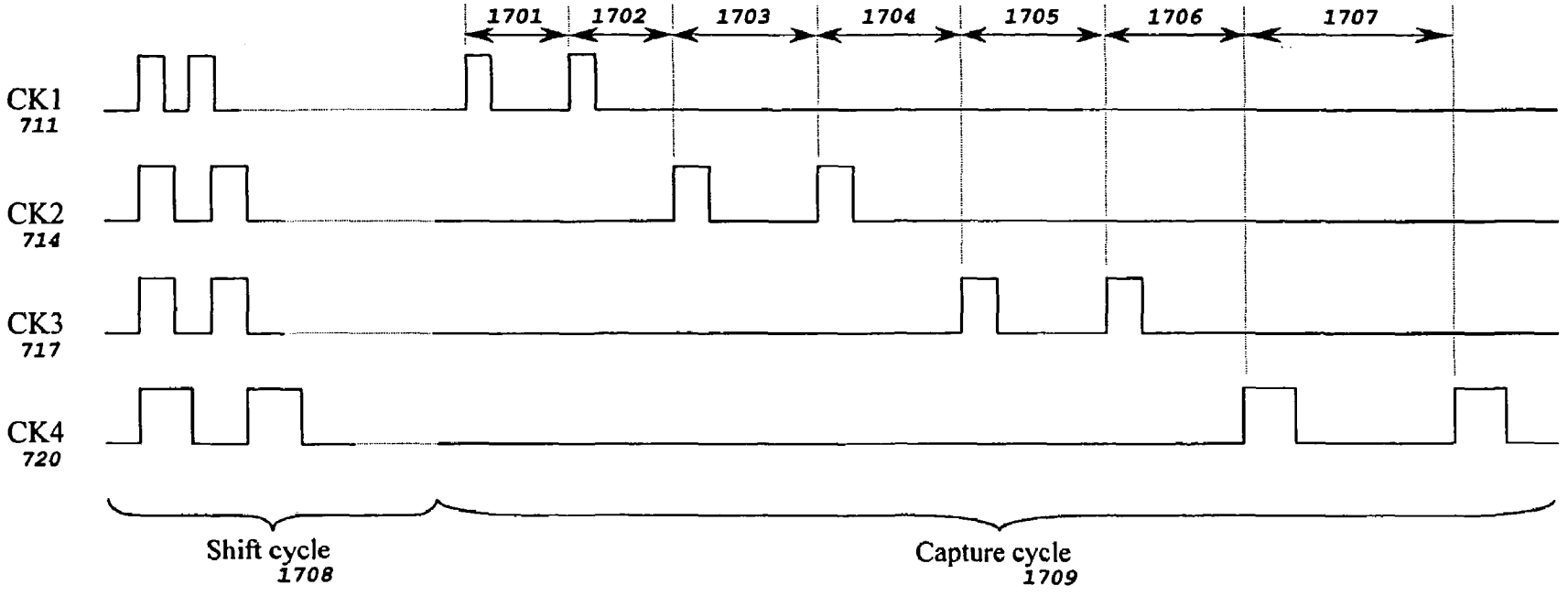
1701
1702
1703
1704
1705
1706
1707
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1708
Capture cycle
1709

FIG. 17

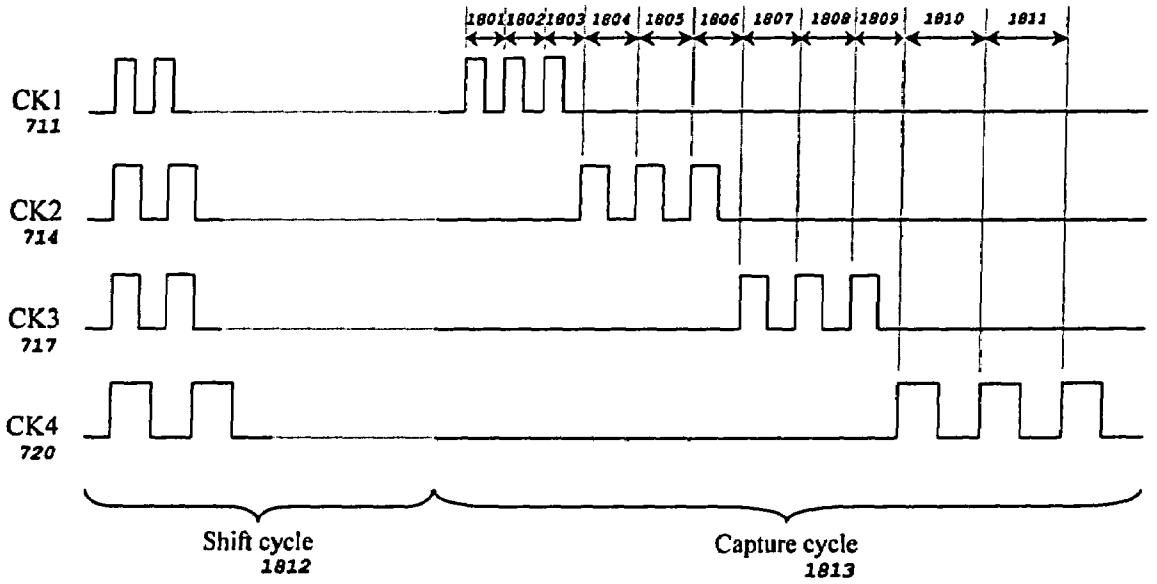
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1812
Capture cycle
1813

FIG. 18

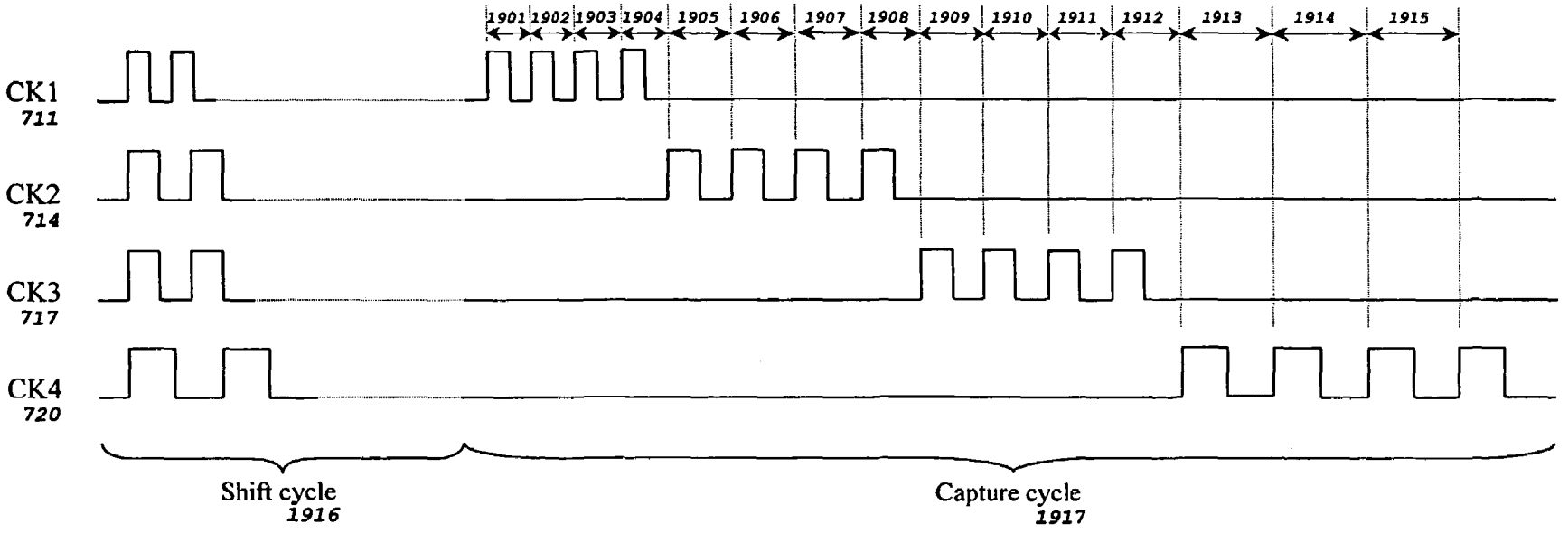
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1916
Capture cycle
1917

FIG. 19

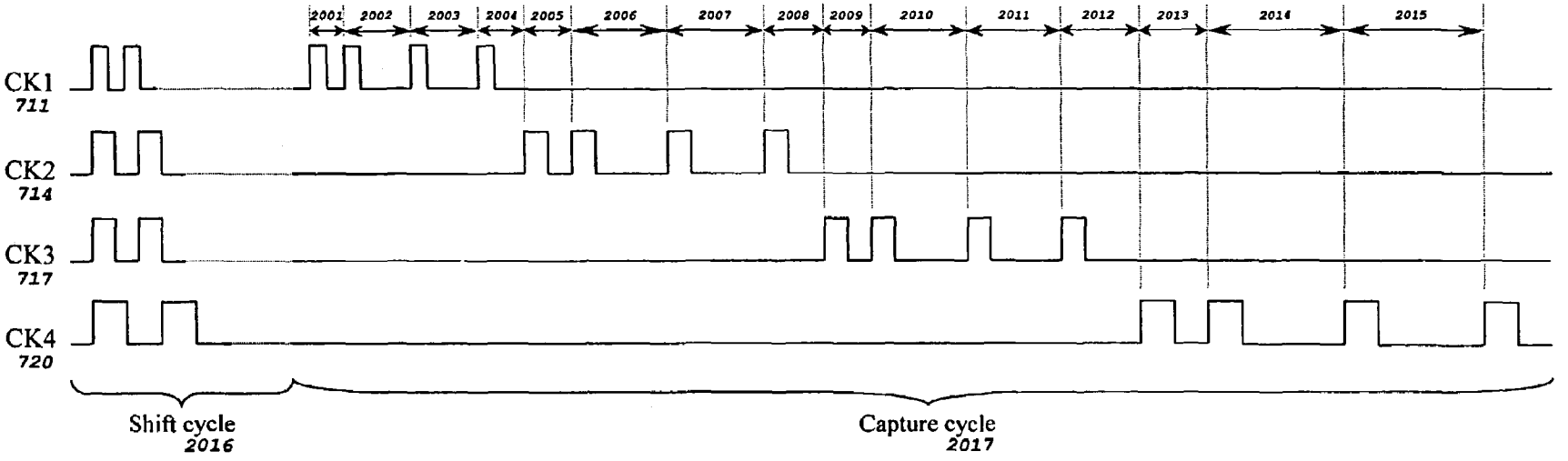
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
2016
Capture cycle
2017

FIG. 20

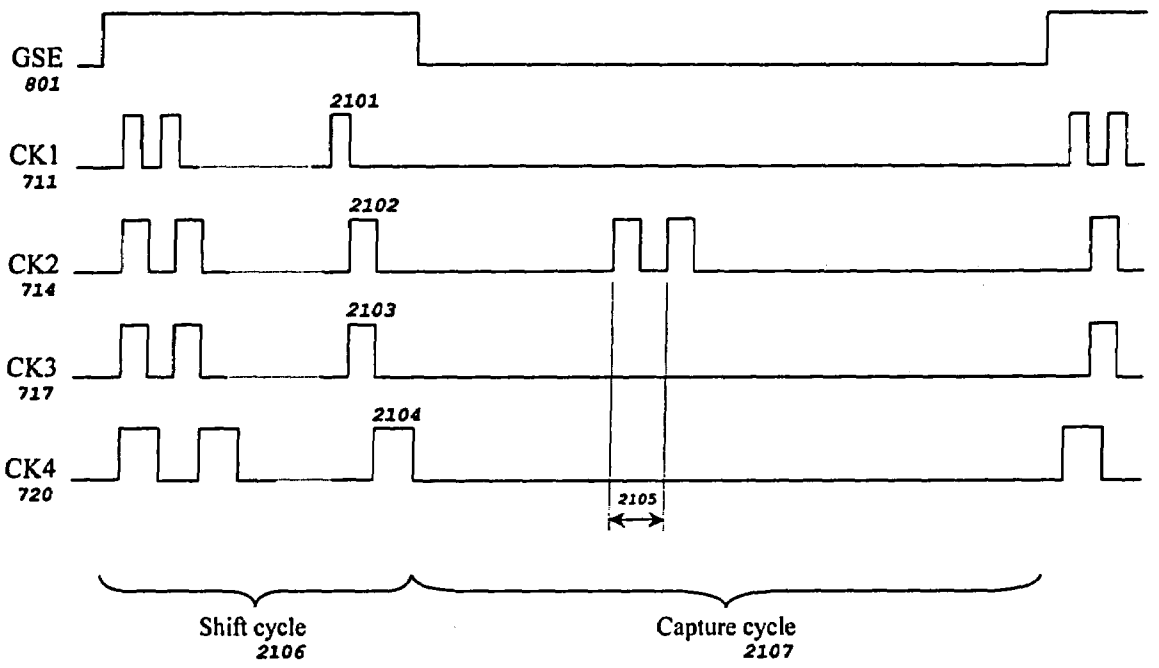
GSE
801
2101
CK1
711
2102
CK2
714
2103
CK3
717
2104
CK4
720
2105
Shift cycle
2106
Capture cycle
2107

FIG. 21

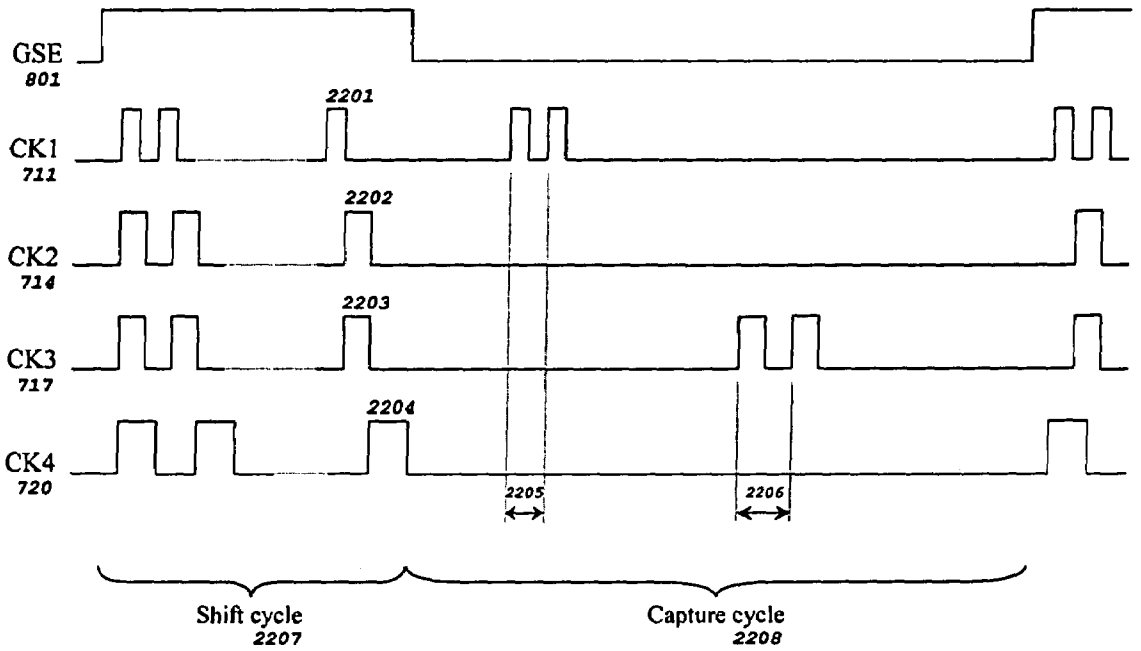
GSE
801
2201
CK1
711
2202
CK2
714
2203
CK3
717
2204
CK4
720
2205
2206
Shift cycle
2207
Capture cycle
2208

FIG. 22

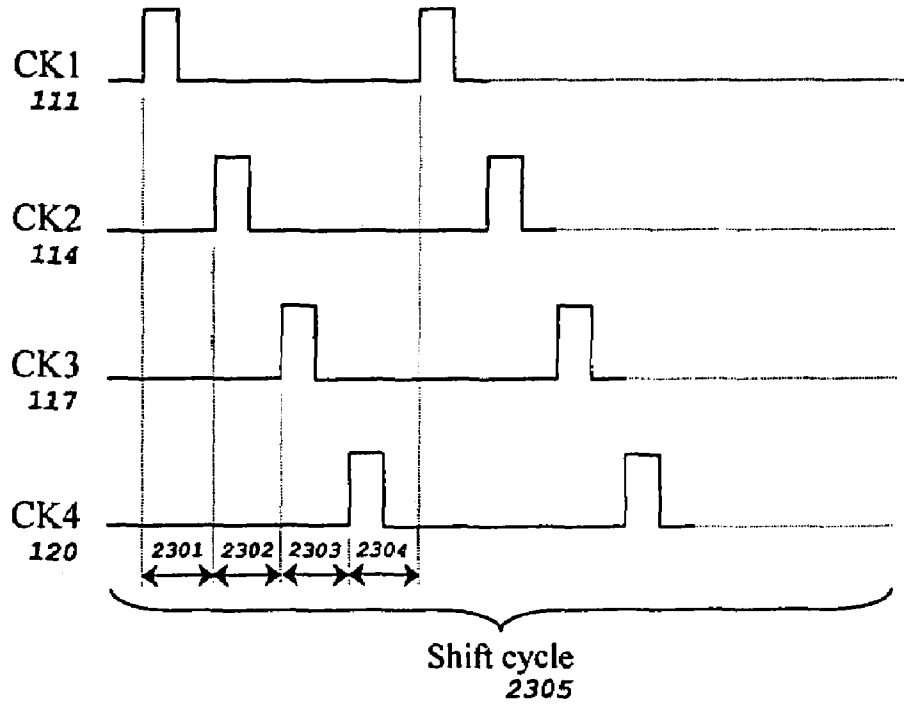
CK1
111
CK2
114
CK3
117
CK4
120
2301
2302
2303
2304
Shift cycle
2305

FIG. 23

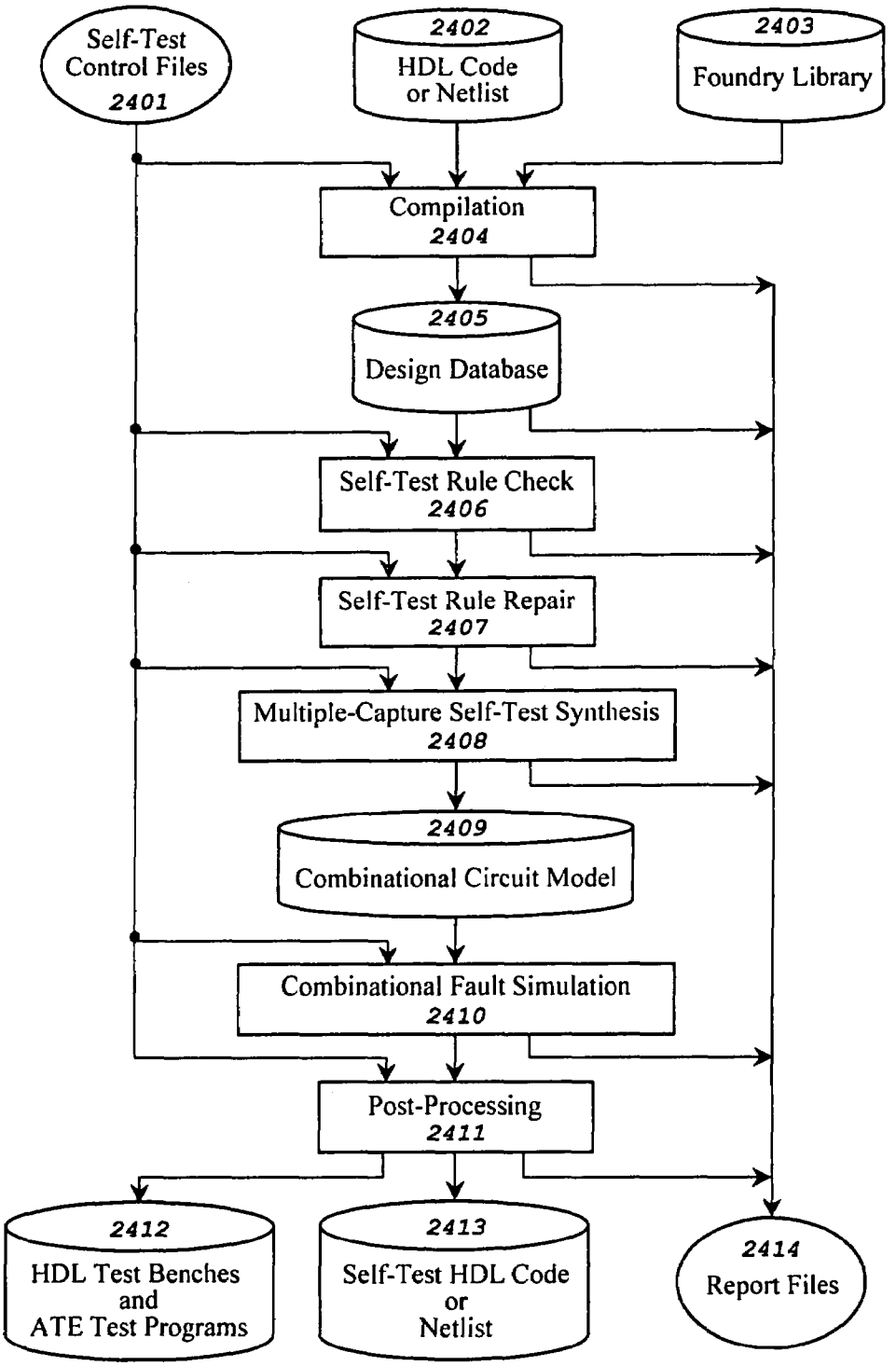
Self-Test Control Files 2401
2402 HDL Code or Netlist
2403 Foundry Library
Compilation 2404
2405 Design Database
Self-Test Rule Check 2406
Self-Test Rule Repair 2407
Multiple-Capture Self-Test Synthesis 2408
2409 Combinational Circuit Model
Combinational Fault Simulation 2410
Post-Processing 2411
2412 HDL Test Benches and ATE Test Programs
2413 Self-Test HDL Code or Netlist
2414 Report Files

FIG. 24

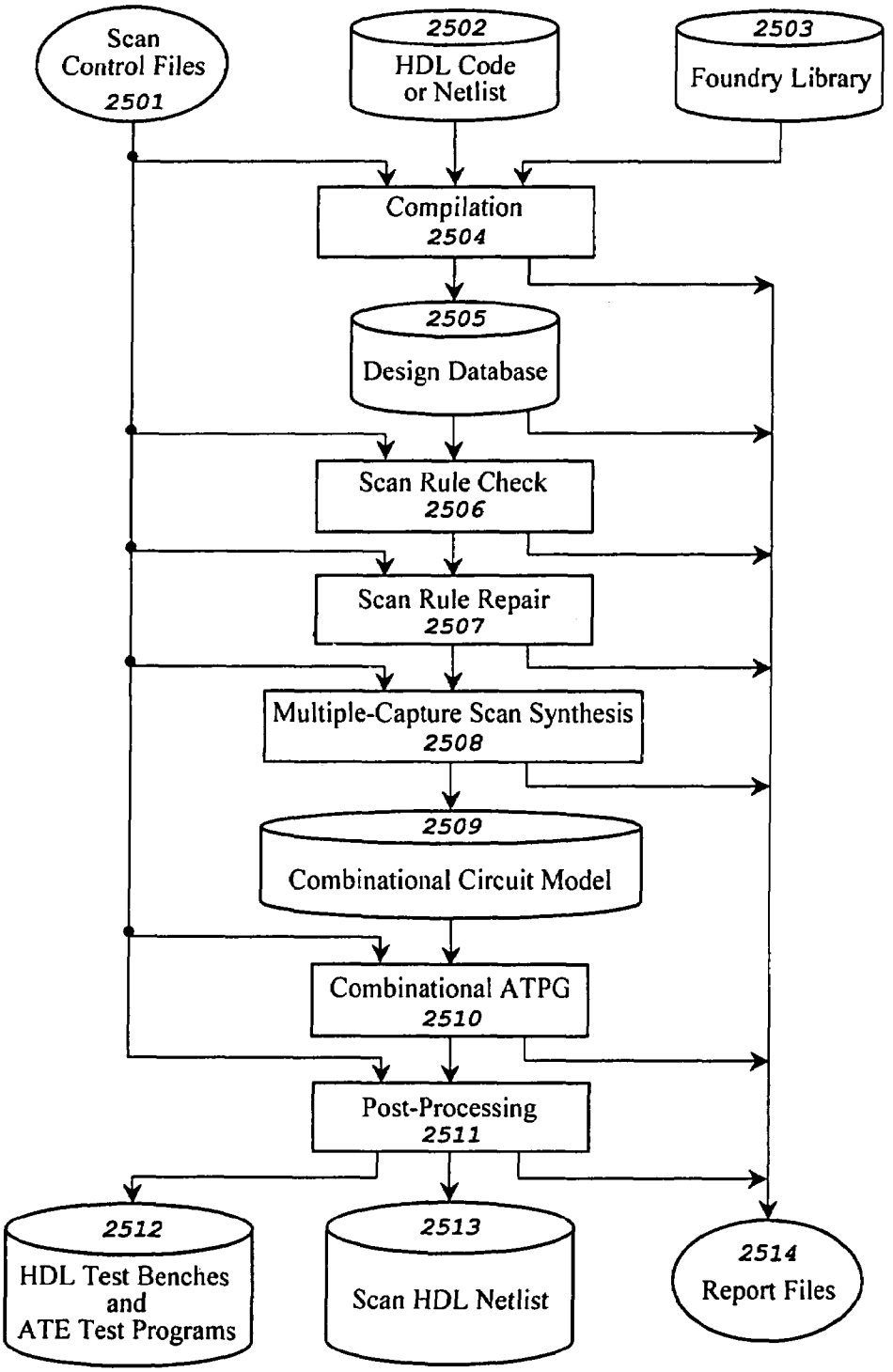
Scan Control Files 2501
2502 HDL Code or Netlist
2503 Foundry Library
Compilation 2504
2505 Design Database
Scan Rule Check 2506
Scan Rule Repair 2507
Multiple-Capture Scan Synthesis 2508
2509 Combinational Circuit Model
Combinational ATPG 2510
Post-Processing 2511
2512 HDL Test Benches and ATE Test Programs
2513 Scan HDL Netlist
2514 Report Files

FIG. 25

COMPUTER-AIDED DESIGN (CAD) MULTIPLE-CAPTURE DFT SYSTEM FOR DETECTING OR LOCATING CROSSING CLOCK-DOMAIN FAULTS

RELATED APPLICATION DATA

The present application is a divisional application of copending application Ser. No. 11/098,703 filed Apr. 5, 2005 which in turn is a divisional application of Ser. No. 10/067,372 filed Feb. 7, 2002, which claims the benefit of provisional application No. 60/268,601 filed Feb. 15, 2001 which is hereby incorporated by reference, and for which priority is claimed for all of the above.

TECHNICAL FIELD

The present invention generally relates to the testing of logic. designs in an integrated circuit or circuit assembly embedded with design-for-test (DFT) techniques. Specifically, the present invention relates to the detection or location of logic faults within each clock domain and logic faults crossing any two clock domains, during self-test or scan-test, in an integrated circuit or circuit assembly.

BACKGROUND OF THE INVENTION

In this specification, the term integrated circuit is used to describe a chip or MCM (multi-chip module) embedded with design-for-test (DFT) techniques. The terms circuit assembly and printed circuit board will be considered interchangeable. The term circuit assembly includes printed circuit boards as well as other types of circuit assem-blies. A circuit assembly is a combination of integrated circuits. The resulting combination is manufactured to form a physical or functional unit.

An integrated circuit or circuit assembly, in general, contains two or more systems clocks, each controlling one module or logic block, called clock domain. Each system clock is either directly coming from a primary input (edge pin/connector) or generated internally. These system clocks can operate at totally unrelated frequencies (clock speeds), at submultiples of each other, at the same frequency but with different clock skews, or at a mix of the above. Due to clock skews among these system clocks, when a DFT technique, such as self-test or scan-test, is employed, it is very likely that faults associated with the function between two clock domains, called crossing clock-domain faults, will become difficult to test. In the worst case, these crossing clock-domain faults when propagating into the receiving clock domain could completely block detection or location of all faults within that clock domain. Thus, in order to solve the fault propagation problem, DFT approaches are proposed to take over control of all system clocks and reconfigure them as capture clocks.

Prior-art DFT approaches in this area to testing crossing clock-domain faults as well as faults within each clock domain centered on using the isolated DFT, ratio'ed DFT, and one-hot DFT techniques. They are all referred to as single-capture DFT techniques, because none of them can provide multiple skewed capture clocks (or an ordered sequence of capture clocks) in each capture cycle during self-test or scan-test.

In using the isolated DFT technique, all boundary signals crossing a clock domain and flowing into the receiving clock domains are completely blocked or disabled by forcing each of them to a predetermined logic value of 0 or 1. See U.S. Pat. No. 6,327,684 issued to Nadeau-Dostie et al. (2001). This approach, in general, can allow all clock domains to be tested in parallel. The major drawbacks of this approach are that it requires insertion of capture-disabled logic in between clock domains and all scan enable signals each associated with one clock domain must be operated at-speed. The design change could take significant efforts and it might impact normal mode operation. Running all scan enable signals at-speed requires routing them as clock signals using layout clock-tree synthesis (CTS). In addition, since boundary signals can traverse through two clock domains in both directions, this approach requires testing crossing clock-domain faults in two or more test sessions. This could substantially increase the test time required and might make the capture-disabled logic even more complex to implement than anticipated.

In using the ratio'ed DFT technique, all clock domains must be operated at sub-multiples of one reference clock. For instance, assume that a design contains 3 clock domains running at 150 MHz, 80 MHz, and 45 MHz, respectively. The 3 clock domains may have to be operated at 150 MHz, 75 MHz, and 37.5 MHz during testing. See U.S. Pat. No. 5,349,587 issued to Nadeau-Dostie et al. (1994). This approach reduces the complexity of testing a multiple-frequency design and avoids potential races or timing violations crossing clock domains. It can also allow testing of all clock domains in parallel. However, due to changes in clock-domain operating frequencies, this approach loses its self-test or scan-test intent of testing multiple-frequency designs at their rated clock speeds (at-speed) and may require significant design and layout efforts on re-timing (or synchronizing) all clock domains. Power consumption could be also another serious problem because all scan cells (memory elements) are triggered simultaneously every few cycles.

In using the one-hot DFT technique, each crossing clock-domain signal flowing into its receiving clock domains must be initialized to or held at a predetermined logic value of 0 or 1 first. This initialization is usually accomplished by shifting in predetermined logic values to all clock domains so that all crossing clock-domain signals are forced to a known state. Testing is then conducted domain-by-domain, thus, called one-hot testing. See U.S. Pat. No. 5,680,543 issued to Bhawmik et al. (1997). The major benefits of using this approach are that it can still detect or locate crossing clock-domain faults and does not need insertion of disabled logic, in particular, in critical paths crossing clock domains. However, unlike the isolated or ratio'ed DFT approach, this approach requires testing of all clock domains in series, resulting in long test time. It also requires significant design and layout efforts on re-timing (or synchronizing) all clock domains.

Two additional prior-art DFT approaches had also been proposed, one for scan-test, the other for self-test. Both approaches are referred to as multiple-capture DFT techniques, because they can provide multiple skewed capture clocks (or an ordered sequence of capture clocks) in each capture cycle during scan-test or self-test.

The first prior-art multiple-capture DFT approach is to test faults within each clock domain and faults between two clock domains in scan-test mode. See U.S. Pat. No. 6,070,260 issued to Buch et al. (2000) and U.S. Pat. No. 6,195,776 issued to Ruiz et al. (2001). These approaches rest on using multiple skewed scan clocks or multiple skew capture events each operating at the same reduced clock speed in an ATE (automatic test equipment) to detect faults. Combinational ATPG (automatic test pattern generation) is used to generate scan-test patterns and ATE test programs are created to detect faults in the integrated circuit. Unfortunately, currently available ATPG tools only assume the application of one clock pulse (clock cycle) to each clock domain. Thus, these approaches can only detect stuck-at faults in scan-test mode.

No prior art using multiple skewed capture clocks were proposed to test delay or stuck-at faults requiring two or more capture clock pulses for full-scan or partial-scan designs.

The second prior-art multiple-capture DFT approach is to test faults within each clock domain and faults between two clock domains in self-test mode. See the paper co-authored by Hetherington et al. (1999). This approach rests on using multiple shift-followed-by-capture clocks each operating at its operating frequency, in a programmable capture window, to detect faults at-speed. It requires clock suppression, complex scan enable (SE) timing waveforms, and shift clock pulses in the capture window to control the capture operation. These shift clock pulses may also need precise timing alignment. As a result, it becomes quite difficult to perform at-speed self-test for designs containing clock domains operated at totally unrelated frequencies, e.g., 133 MHz and 60 MHz.

Thus, there is a need for an improved method, apparatus, or computer-aided design (CAD) system that allows at-speed or slow-speed testing of faults within clock domains and between any two clock domains using a simple multiple-capture DFT technique. The method and apparatus of the present invention will control the multiple-capture operations of the capture clocks in self-test or scan-test mode. It does not require using shift clock pulses in the capture window, inserting capture-disabled logic in normal mode, applying clock suppression on capture clock pulses, and programming complex timing waveforms on scan enable (SE) signals. In addition, the CAD system of the present invention further comprises the computer-implemented steps of performing multiple-capture self-test or scan synthesis, combinational fault simulation, and combinational ATPG that are currently unavailable in the CAD field using multiple-capture DFT techniques.

SUMMARY OF THE INVENTION

Accordingly, a primary objective of the present invention is to provide an improved multiple-capture DFT system implementing the multiple-capture DFT technique. Such a DFT system will comprise a method or apparatus for allowing at-speed/slow-speed detection or location of faults within all clock domains and faults crossing clock domains in an integrated circuit or circuit assembly. In the present invention, the method or apparatus can be realized and placed inside or external to the integrated circuit or circuit assembly.

A computer-aided design (CAD) system that synthesizes such a DFT system and generates desired HDL test benches and ATE test programs is also included in the present invention. A hardware description language (HDL) is used to represent the integrated circuit includes, but is not limited to, Verilog or VHDL. An ATE is an IC tester or any equipment that realizes the multiple-capture DFT system and is external to the integrated circuit or circuit assembly under test.

The present invention focuses on multiple-capture DFT systems for self-test and scan-test. In a self-test environment, a self-test cycle often comprises 3 major operations: shift, capture, and compact. The shift and compact operations can occur concurrently during each self-test cycle. In order to increase the circuit's fault coverage, it is often necessary to include scan-test cycles to perform top-up ATPG. A scan-test cycle often comprises 3 major operations in a scan-test environment: shift, capture, and compare. The shift and compare operations can occur concurrently during each scan-test cycle. In a mixed self-test and scan-test environment, the scan-test cycle may execute a compact operation rather than the compare operation. Thus, in the present invention, a self-test cycle further comprises the shift, capture, and compare operations, and a scan-test cycle further comprises the shift, capture, and compact operations.

The multiple-capture DFT system of the present invention further comprises any method or apparatus for executing the shift and compact or shift and compare operations concurrently during each self-test or scan-test cycle. It is applicable to test any integrated circuit or circuit assembly which contains N clock domains, where N>1. Each capture clock controls one clock domain and can operate at its rated clock speed (at-speed) or at a reduced clock speed (slow-speed), when desired.

During the shift operation, the multiple-capture DFT system first generates and shifts in (loads) N pseudorandom or predetermined stimuli to all scan cells within all clock domains, concurrently. The shifting frequency is irrelevant to at-speed testing. Depending on needs, a slower frequency can be used to reduce power consumption and a faster frequency can be used to reduce the test application time. The multiple-capture DFT system must wait until all stimuli have been loaded or shifted into all scan cells. By that time, all scan enable (SE) signals each associated with one clock domain shall switch from the shift operation to the capture operation. After the capture operation is completed, all scan enable (SE) signals shall switch from the capture operation to the shift operation. One global scan enable (GSE) signal can be simply used to drive these scan enable signals.

The multiple-capture DFT system of the present invention further comprises any method or apparatus for performing the shift operation at any selected clock speed within each clock domain and using only one global scan enable (GSE) signal to drive all scan enable (SE) signals for at-speed or slow-speed testing. The GSE signal can be also operated at its selected reduced clock speed. Thus, there is no need to route these SE signals as clock signals using layout clock tree synthesis (CTS). This invention applies to any self-test or scan-test method that requires multiple capture clock pulses (without including shift clock pulses) in the capture cycle.

After the shift operation is completed, an ordered sequence of capture clocks is applied to all clock domains. During the capture operation, each ordered sequence contains N capture clocks of which only one or a few will be active at one time. There are no shift clock pulses present within each capture cycle. Testing of delay faults at-speed is now performed by applying two consecutive capture clock pulses (double captures) rather than using the shift-followed-by-capture clock pulses. Performing multiple captures in the capture cycle reduces the risk of delay test invalidation and false paths that might occur due to illegal states in scan cells resulting from filling them with pseudorandom or predetermined stimuli.

In the present invention, the multiple-capture DFT system uses a daisy-chain clock-triggering or token-ring clock-enabling technique to generate and order capture clocks one after the other. One major benefit of using this approach is that the test results are repeatable no matter what clock speed will be used for each capture clock. The problem is it could be difficult to precisely control the relative clock delay between two adjacent capture clocks for testing delay faults between clock domains.

As an example, assume that the capture cycle contains 4 capture clocks, CK**1**, CK**2**, CK**3**, and CK**4**. (Please refer to FIGS. **3** and **10** in the DETAILED DESCRIPTION OF THE DRAWINGS section for further descriptions). The daisy-chain clock-triggering technique implies that completion of the shift cycle triggers the GSE signal to switch from shift to capture cycle which in turn triggers CK**1**, the rising edge of the last CK**1** pulse triggers CK**2**, the rising edge of the last

CK2 pulse triggers CK3, and the rising edge of the last CK3 pulse triggers CK4. Finally, the rising edge of the last CK4 pulse triggers the GSE signal to switch from capture to shift cycle.

The token-ring clock-enabling technique implies that completion of the shift cycle enables the GSE signal to switch from shift to capture cycle which in turn enables CK1, completion of CK1 pulses enables CK2, completion of CK2 pulses enables CK3, and completion of CK3 pulses enables CK4. Finally, completion of CK4 pulses enables the GSE signal to switch from capture to shift cycle.

The only difference between these two techniques is that the former uses clock edges to trigger the next operation, the latter uses signal levels to enable the next operation. In practice, a mixed approach can be employed. Since a daisy-chain or token-ring approach is used, the multiple-capture DFT system allows testing of any frequency domain at a reduced clock speed when this particular frequency domain cannot operate at-speed. This is very common in testing high-speed integrated circuits, such as microprocessors and networking chips, where different clock speeds of chips are sold at different prices. In addition, due to its ease of control, this approach further allows at-speed scan-test simply using internally reconfigured capture clocks. Thus, a low-cost tester (ATE) can be used for at-speed scan-test, in addition to at-speed self-test.

The multiple-capture DFT system in the present invention further comprises applying an ordered sequence of capture clocks and operating each capture clock at its selected clock speed in the capture operation (cycle). The ordered sequence of capture clocks is applied to the circuit under test one-by-one using the daisy-chain clock-triggering or token-ring clock-enabling technique. The order of these capture clocks is further programmable, when it's required to increase the circuit's fault coverage. Each capture clock can be also disabled or chosen to facilitate fault diagnosis. In addition, when two clock domains do not interact with each other, they can be tested simultaneously to shorten the capture cycle time.

Each capture clock of the present invention further comprises one or more clock pulses. The number of clock pulses is further programmable. When self-test is employed, the multiple-capture DFT system is usually placed inside the integrated circuit and, thus, all capture clocks are generated internally. When scan-test is employed, the multiple-capture DFT system is usually resided in an ATE and, thus, all capture clocks are controlled externally. However, for at-speed scan-test, it's often required to capture output responses using its respective operating frequency within each clock domain. The present invention further comprises any method or apparatus for allowing use of internally-generated or externally-controlled capture clocks for at-speed scan-test or self-test.

After the capture operation is completed, all output responses captured at all scan cells are compacted internally to signatures or shifted out to the multiple-capture DFT system for direct comparison. The compact or compare operation occurs concurrently with the shift operation, and the process of shift, capture, and compact/compare operations shall continue until a predetermined limiting criteria, such as completion of all self-test or scan-test cycles, is reached. Finally, the multiple-capture DFT system will compare the signatures against expected signatures when the compact operation is employed during self-test or scan-test. Such comparison can be done either in the integrated circuit with a built-in comparator or in an ATE by shifting the final signatures out for analysis.

In the present invention, both self-test and scan-test techniques are employed to detect or locate stuck-at and delay faults. The stuck-at faults further comprise other stuck-type faults, such as open and bridging faults. The delay faults further comprise other non-stuck-type delay faults, such as transition (gate-delay), multiple-cycle delay, and path-delay faults. In addition, each scan cell can be a multiplexed D flip-flop or a level sensitive latch, and the integrated circuit or circuit assembly under test can be a full-scan or partial-scan design.

In general, it is only required to apply one clock pulse and two consecutive clock pulses to test stuck-at faults and delay faults within one clock domain, respectively. Multiple-cycle paths present within one clock domain and between clock domains, however, require waiting for a number of clock cycles for capturing. To test multiple-cycle paths within clock domains, the present invention further comprise applying only one clock pulse to test these multiple-cycle paths within each clock domain by reducing the frequency of that domain's capture clock speed to the level where only paths of equal cycle latency (cycle delays) are captured at its intended rated clock speed one at a time. To test multiple-cycle paths between two clock domains, the present invention further comprise adjusting the relative clock delay along the paths to the level where the crossing-boundary multiple-cycle paths are captured at its intended rated clock speed.

To summarize, the present invention centers on using one global scan enable (GSE) signal for driving all scan enable (SE) signals at a reduced clock speed and applying an ordered sequence of capture clocks for capturing output responses in both self-test and scan-test modes. The present invention assumes that the integrated circuit or circuit assembly must contain two or more clock domains each controlled by one capture clock. During self-test, each capture clock shall contain one or more clock pulses, and during scan-test, one of the capture clocks must contain two or more clock pulses.

Due to its ease of control on the scan enable and capture clock signals, the multiple-capture DFT system of the present invention can now be easily realized by an apparatus and synthesized using computer-aided design (CAD) tools. The present invention further comprises such a CAD system for synthesizing the apparatus and verifying its correctness using combinational fault simulation and combinational ATPG in self-test or scan-test mode.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, advantages and features of the invention will become more apparent when considered with the following specification and accompanying drawings wherein:

FIG. **1** shows an example full-scan or partial-scan design with 4 clock domains and 4 system clocks, where a multiple-capture DFT system in accordance with the present invention is used to detect or locate stuck-at faults at a reduced clock speed in self-test or scan-test mode.

FIG. **2** shows a multiple-capture DFT system with multiple PRPG-MISR pairs, in accordance with the present invention, which is used at a reduced clock speed in self-test mode to detect or locate stuck-at faults in the design given in FIG. **1**.

FIG. **3** shows a timing diagram of the full-scan design given in FIG. **1**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and stuck-at faults crossing clock domains in self-test mode. The chain of control events is also shown.

FIG. **4** shows a timing diagram of the full-scan design given in FIG. **1**, in accordance with the present invention, where a shortened yet ordered sequence of capture clocks is

used to detect or locate stuck-at faults within each clock domain and stuck-at faults crossing clock domains in self-test mode.

FIG. **5** shows a timing diagram of the full-scan design given in FIG. **1**, in accordance with the present invention, where an expanded yet ordered sequence of capture clocks is used to detect or locate other stuck-type faults within each clock domain and other stuck-type faults crossing clock domains in self-test or scan-test mode.

FIG. **6** shows a timing diagram of the partial-scan design given in FIG. **1**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **7** shows an example full-scan or partial-scan design with 4 clock domains and 4 system clocks, where a multiple-capture DFT system in accordance with the present invention is used to detect or locate stuck-at, delay, and multiple-cycle delay faults at its desired clock speed in self-test or scan-test mode.

FIG. **8** shows a multiple-capture DFT system with multiple PRPG-MISR pairs, in accordance with the present invention, which is used at its desired clock speed in self-test or scan-test mode to detect or locate stuck-at, delay, and multiple-cycle delay faults in the design given in FIG. **7**.

FIG. **9** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and stuck-at faults crossing clock domains in self-test mode.

FIG. **10** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode. The chain of control events is also shown.

FIG. **11** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where a shortened yet ordered sequence of capture clocks is used to detect or locate delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **12** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and delay faults crossing clock domains in self-test or scan-test mode.

FIG. **13** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate delay faults within each clock domain and delay faults crossing clock domains in self-test or scan-test mode.

FIG. **14** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where a reordered sequence of capture clocks is used to detect or locate delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **15** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an expanded yet ordered sequence of capture clocks is used to detect or locate additional delay faults within each clock domain and additional stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **16** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate 2-cycle delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **17** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate 2-cycle delay faults within each clock domain and 2-cycle delay faults crossing clock domains in self-test or scan-test mode.

FIG. **18** shows a timing diagram of the partial-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **19** shows a timing diagram of the partial-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **20** shows a timing diagram of the partial-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate 2-cycle delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **21** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where the capture clock CK**2** during the capture cycle is chosen to diagnose faults captured by CK**2** in self-test or scan-test mode.

FIG. **22** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where the capture clocks CK**1** and CK**3** during the capture cycle are chosen to diagnose faults captured by CK**1** and CK**3** in self-test or scan-test mode.

FIG. **23** shows a timing diagram of the full-scan design given in FIG. **1**, in accordance with the present invention, where all capture clocks during the shift cycle are skewed to reduce power consumption.

FIG. **24** shows a multiple-capture CAD system in accordance with the present invention, where a CAD system is used to implement the multiple-capture DFT technique on a full-scan or partial-scan design in self-test mode.

FIG. **25** shows a multiple-capture CAD system in accordance with the present invention, where a CAD system is used to implement the multiple-capture DFT technique on a full-scan or partial-scan design in scan-test mode.

DETAILED DESCRIPTION OF THE DRAWINGS

The following description is of presently contemplated as the best mode of carrying out the present invention. This description is not to be taken in a limiting sense but is made merely for the purpose of describing the principles of the invention. The scope of the invention should be determined by referring to the appended claims.

FIG. **1** shows an example full-scan or partial-scan design with a multiple-capture DFT system, of one embodiment of the invention. The design **133** contains 4 clock domains, CD**1** **102** to CD**4** **105**, and 4 system clocks, CK**1** **111** to CK**4** **120**. Each system clock controls one clock domain. CD**1** **102** and CD**2** **103** talk to each other via a crossing clock-domain logic block CCD**1** **106**; CD**2** **103** and CD**3** **104** talk to each other via a crossing clock-domain logic block CCD**2** **107**; and CD**3** **104** and CD**4** **105** talk to each other via a crossing clock-domain logic block CCD**3** **108**.

The 4 clock domains, CD**1** **102** to CD**4** **105**, are originally designed to run at 150 MHz, 100 MHz, 100 MHz, and 66 MHz, respectively. However, in this example, since a DFT (self-test or scan-test) technique is only employed to detect or locate stuck-at faults in the design **133**, all system clocks, CK**1** **111** to CK**4** **120**, are reconfigured to operate at 10 MHz. The reconfigured system clocks are called capture clocks.

During self-test or scan-test, the multiple-capture DFT system **101** will take over the control of all stimuli, **109**, **112**, **115**, and **118**, all system clocks, CK**1** **111** to CK**4** **120**, and all output responses, **110**, **113**, **116**, and **119**.

During the shift operation, the multiple-capture DFT system **101** first generates and shifts pseudorandom or predetermined stimuli through **109**, **112**, **115**, and **118** to all scan cells SC in all scan chains SCN within the **4** clock domains, CD**1** **102** to CD**4** **105**, simultaneously. The multiple-capture DFT system **101** shall wait until all stimuli, **109**, **112**, **115**, and **118**, have been shifted into all scan cells SC. It should be noted that, during the shift operation, the capture clock can be operated either at its rated clock speed (at-speed) or at a desired clock speed.

After the shift operation is completed, an ordered sequence of capture clocks is applied to all clock domains, CD**1** **102** to CD**4** **105**. During the capture operation, each capture clock can operate at its rated clock speed (at-speed) or at a reduced speed (slow-speed), and can be generated internally or controlled externally. In this example, all system clocks, CK**1** **111** to CK**4** **120**, are reconfigured to operate at a reduced frequency of 10 MHz.

After the capture operation is completed, the output responses captured at all scan cells SC are shifted out through responses **110**, **113**, **116**, and **119** to the multiple-capture DFT system **101** for compaction during the compact operation or direct comparison during the compare operation.

Based on FIG. **1**, the timing diagrams given in FIGS. **3** to **6** are used to illustrate that, by properly ordering the sequence of capture clocks and by adjusting relative inter-clock delays, stuck-at faults within each clock domain and crossing clock domains can be detected or located in self-test or scan-test mode. Please note that different ways of ordering the sequence of capture clocks and adjusting relative inter-clock delays will result in different faults to be detected or located.

FIG. **2** shows a multiple-capture DFT system with three PRPG-MISR pairs, of one embodiment of the invention, used to detect or locate stuck-at faults in the design **133** given in FIG. **1** in self-test mode.

Pseudorandom pattern generators (PRPGs), **211** to **213**, are used to generate pseudorandom patterns. Phase shifters, **214** to **216**, are used to break the dependency between different outputs of the PRPGs. The bit streams coming from the phase shifters become test stimuli, **109**, **112**, **115**, and **118**.

Space compactors, **217** to **219**, are used to reduce the number of bit streams in test responses, **110**, **113**, **116**, and **119** shifted out of CD**1** **102**, CD**2** **103**, CD**3** **104**, and CD**4** **105**, respectively. Space compactors are optional and are only used when the overhead of a MISR becomes a concern. The outputs of the space compactors are then compressed by multiple input signature registers (MISRs), **220** to **222**. The contents of MISRs after all test stimuli are applied become signatures, **236** to **238**. The signatures are then be compared by comparators, **223** to **225**, with corresponding expected values. The error indicator **226** is used to combine the individual pass/fail signals, **242** to **244**, a global pass/fail signal **245**. Alternatively, the signatures in MISRs **220** to **222** can be shifted to the outside of the design for comparison through a single scan chain composed of elements **223**, **239**, **224**, **240**, **225**, and **241**.

The central self-test controller **202** controls the whole test process by manipulating individual scan enable signals, **204** to **207**, and by reconfiguring capture clocks, CK**1** **111** to CK**4** **120**. Especially, the scan enable signals, **204** to **207**, can be controlled by one global scan enable signal GSE **201**, which can be a slow signal in that it does not have to settle down in half of the cycle of any clock applied to any clock domain. Some additional control signals **203**, connected to **208**, **209** and **210**, are needed to conduct other control tasks.

The clock domains **103** and **104**, which are operated at the same frequency, share the same pair of PRPG **212** and MISR **221**. It should be noted that the skew between the clocks CK**2** **114** and CK**3** **117** should be properly managed to prevent any timing violations during the shift operation and any races during the capture operation.

All storage elements in PRPGs, **211** to **213**, and MISRs, **220** to **222**, can be connected into a scan chain through paths **246** to **252** from which predetermined patterns can be shifted in for reseeding and computed signatures can be shifted out for analysis. This configuration helps in increasing fault coverage and in facilitating fault diagnosis.

FIG. **3** shows a timing diagram of a full-scan design given in FIG. **1**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test mode. The timing diagram **300** shows the sequence of waveforms of the 4 capture clocks, CK**1** **111** to CK**4** **120**, operating at the same frequency.

During each shift cycle **310**, a series of pulses of 10 MHz are applied through capture clocks, CK**1** **111** to CK**4** **120**, to shift stimuli to all scan cells within all clock domains, CD**1** **102** to CD**4** **105**.

During each capture cycle **311**, 4 sets of capture clock pulses are applied in the following order: First, one capture pulse is applied to CK**1** **111** to detect or locate stuck-at faults within the clock domain CD**1** **102**. Second, one capture pulse is applied to CK**2** **114** to detect or locate stuck-at faults within the clock domain CD**2** **103**. Third, one capture pulse is applied to CK**3** **117** to detect or locate stuck-at faults within the clock domain CD**3** **104**. Fourth, one capture pulse is applied to CK**4** **120** to detect or locate stuck-at faults within the clock domain CD**4** **105**.

In addition, the stuck-at faults which can be reached from lines **121**, **125**, and **129** in the crossing clock-domain logic blocks CCD**1** **106** to CCD**3** **108**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **307** between the rising edge of the capture pulse of CK**1** **111** and the rising edge of the capture pulse of CK**2** **114** must be adjusted so that no races or timing violations would occur while the output responses **123** are captured through the crossing clock-domain logic block CCD**1** **106**.

The same principle applies to the relative clock delay **308** between CK**2** **114** and CK**3** **117**, and the relative clock delay **309** between CK**3** **117** and CK**4** **120** for capturing output responses, **127** and **131**, through CCD**2** **107** and CCD**3** **108**, respectively.

It should be noticed that, generally, during each shift cycle, any capture clock is allowed to operate at its desired or a reduced clock speed. In addition, it is not necessary that all capture clocks must operate at the same clock speed. Furthermore, to reduce peak power consumption during the shift cycle, all capture clocks can be skewed so that at any given time only scan cells within one clock domain can change states. One global scan enable signal GSE **201**, operated at a

reduced clock speed, can also be used, when requested, to switch the test operation from the shift cycle to the capture cycle, and vice versa.

The daisy-chain clock-triggering technique is used to generate and order the sequence of capture clocks one after the other in the following way: The rising edge of the last pulse in the shift cycle triggers the event **301** of applying 0 to the global scan enable GSE **201**, switching the test operation from the shift cycle to the capture cycle. The falling edge of GSE **201** triggers the event **302** of applying one capture pulse to CK**1** **111**. Similarly, the rising edge of the capture pulse of CK**1** **111** triggers the event **303** of applying one capture pulse to CK**2** **114**, the rising edge of the capture pulse of CK**2** **114** triggers the event **304** of applying one capture pulse to CK**3** **117**, and the rising edge of the capture pulse of CK**3** **117** triggers the event **305** of applying one capture pulse to CK**4** **120**. Finally, the rising edge of the capture pulse of CK**4** **120** triggers the event **306** of applying 1 to the global scan enable GSE **201**, switching the test operation from the capture cycle to the shift cycle. This daisy-chain clock-triggering technique is also used to order the sequence of capture clocks in FIGS. **4** to **6**.

FIG. **4** shows a timing diagram of a full-scan design given in FIG. **1**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with a shortened yet ordered sequence of capture clocks in self-test mode. The timing diagram **400** shows the sequence of waveforms of the 4 capture clocks, CK**1** **111** to CK**4** **120**, operating at the same frequency.

During each shift cycle **402**, a series of clock pulses of 10 MHz are applied through capture clocks, CK**1** **111** to CK**4** **120**, to shift stimuli to all scan cells within all clock domains, CD**1** **102** to CD**4** **105**.

During each capture cycle **403**, two sets of capture clock pulses are applied in the following order: First, one capture pulse is applied to CK**1** **111** and CK**3** **117** simultaneously to detect or locate stuck-at faults within the clock domain CD**1** **102** and CD**3** **104**, respectively. Second, one capture pulse is applied to CK**2** **114** and CK**4** **120** simultaneously to detect or locate stuck-at faults within the clock domain CD**2** **103** and CD**4** **105**, respectively.

In addition, the stuck-at faults which can be reached from lines **121**, **128**, and **129** in the crossing clock-domain logic blocks CCD**1** **106** to CCD**3** **108**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **401** between the rising edge of the capture pulse for CK**1** **111** and CK**3** **117** and the rising edge of the capture pulse for CK**2** **114** and CK**4** **120**, must be adjusted so that no races or timing violations would occur while the output responses, **123**, **126**, and **131**, are captured through the crossing clock-domain logic blocks CCD**1** **106** to CCD**3** **108**.

FIG. **5** shows a timing diagram of a full-scan design in FIG. **1** of one embodiment of the invention for detecting or locating other stuck-type faults within each clock domain and other stuck-type faults crossing clock domains with an expanded yet ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **500** shows the sequence of waveforms of the 4 capture clocks, CK**1** **111** to CK**4** **120**, operating at the same frequency.

During each shift cycle **503**, a series of clock pulses of 10 MHz are applied through capture clocks, CK**1** **111** to CK**4** **120**, to shift stimuli to all scan cells within all clock domains, CD**1** **102** to CD**4** **105**.

During each capture cycle **504**, two sets of capture clock pulses are applied in the following order: First, two capture pulses are applied to CK**1** **111** and CK**3** **117**, simultaneously.

Second, one capture pulse is applied to CK**2** **114** and CK**4** **120**, simultaneously. Stuck-at faults in all crossing clock-domain combinations, from **121** to **123**, from **124** to **122**, from **125** to **127**, from **128** to **126**, from **129** to **131**, from **132** to **130**, can be detected or located if the following condition is satisfied: The relative clock delay **501** between the rising edge of the first capture pulse of CK**1** **111** and CK**3** **117** and the rising edge of the capture pulse of CK**2** **114** and CK**4** **120** must be adjusted so that no races or timing violations would occur while the output responses **123**, **126**, and **131** are captured through the crossing clock-domain logic block CCD**1** **106** to CCD**3** **108**, respectively. The relative clock delay **502** between the rising edge of the capture pulse of CK**2** **114** and CK**4** **120** and the second capture pulse of CK**1** **111** and CK**3** **117** must be adjusted so that no races or timing violations would occur while the output responses **122**, **127**, and **130** are captured through the crossing clock-domain logic block CCD**1** **106** to CCD**3** **108**, respectively.

FIG. **6** shows a timing diagram of a feed-forward partial-scan design given in FIG. **1**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with a shortened yet ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that the clock domains CD**1** **102** to CD**4** **105** contain a number of un-scanned storage cells that form a sequential depth of no more than 2. The timing diagram shows the sequence of waveforms of the 4 capture clocks, CK**1** **111** to CK**4** **120**, operating at the same frequency.

During each shift cycle **606**, a series of clock pulses of 10 MHz are applied through capture clocks, CK**1** **111** to CK**4** **120**, to shift stimuli to all scan cells within all clock domains, CD**1** **102** to CD**4** **105**.

During each capture cycle **607**, two sets of capture clock pulses are applied in the following order: First, three pulses of 10 MHz, two being functional pulses and one being a capture pulse, are applied to CK**1** **111** and CK**3** **117** simultaneously to detect or locate stuck-at faults within the clock domain CD**1** **102** and CD**3** **104**, respectively. Second, three pulses of 10 MHz, two being functional pulses and one being a capture pulse, are applied to CK**2** **114** and CK**4** **120** simultaneously to detect or locate stuck-at faults within the clock domain CD**2** **103** and CD**4** **105**, respectively.

In addition, the stuck-at faults which can be reached from lines **121**, **128**, and **129** in the crossing clock-domain logic blocks CCD**1** **106** to CCD**3** **108**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **603** between the rising edge of the capture pulse for CK**1** **111** and CK**3** **117** and the rising edge of the capture pulse for CK**2** **114** and CK**4** **120** must be adjusted so that no races or timing violations would occur while the output responses, **123**, **126**, and **131**, are captured through the crossing clock-domain logic blocks CCD**1** **106** to CCD**3** **108**.

FIG. **7** shows an example full-scan or partial-scan design with a multiple-capture DFT system **701**, of one embodiment of the invention. The design **733** is the same as the design **133** given in FIG. **1**. Same as in FIG. **1**, the 4 clock domains, CD**1** **702** to CD**4** **705**, are originally designed to run at 150 MHz, 100 MHz, 100 MHz, and 66 MHz, respectively. The only difference from FIG. **1** is that these clock frequencies will be used directly without alternation in order to implement at-speed self-test or scan-test for stuck-at, delay, and multiple-cycle delay faults within each clock domain and crossing clock domains. In self-test or scan-test mode, the multiple-capture DFT system **701** will take over the control of all

stimuli, **709**, **712**, **715** and **718**, all system clocks, CK**1** **711** to CK**4** **720**, and all output responses, **710**, **713**, **716** and **719**.

Based on FIG. **7**, the timing diagrams given in FIGS. **9** to **20** are used to illustrate that, by properly ordering the sequence of capture pulses and by adjusting relative inter-clock delays, the at-speed detection or location of stuck-at, delay, and multiple-cycle delay faults within each clock domain and crossing clock domains can be achieved in self-test or scan-test mode. Please note that different ways of ordering the sequence of capture pulses and adjusting relative inter-clock delays will result in different faults to be detected or located.

FIG. **8** shows a multiple-capture DFT system with three PRPG-MISR pairs, of one embodiment of the invention, used in self-test or scan-test mode to detect or locate stuck-at, delay, and multiple-cycle delay faults in the design given in FIG. **7**. The composition and operation of the multiple-capture DFT system is basically the same as the one given in FIG. **2**. There are two major differences: One is that, in this example, the original clock frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are used directly without alternation in order to implement at-speed self-test or scan-test. The other is that more care needs to be taken in the physical design of scan chains, etc., in this example.

The clock domains **703** and **704**, which are operated at the same frequency, share the same pair of PRPG **812** and MISR **821**. It should be noted that the skew between the clocks CK**2** **714** and CK**3** **717** should be properly managed to prevent any timing violations during the shift operation and any races during the capture operation.

All storage elements in PRPGs, **811** to **813**, and MISRs, **820** to **822**, can be connected into a scan chain from which predetermined patterns can be shifted in for reseeding and computed signatures can be shifted out for analysis. This configuration helps in increasing fault coverage and in facilitating fault diagnosis.

FIG. **9** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test mode. The timing diagram **900** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies. This timing diagram is basically the same as the one given in FIG. **3** except the capture clocks, CK**1** **711** to CK**4** **720**, run at 150 MHz, 100 MHz, 100 MHz, and 66 MHz, respectively, in both shift and capture cycles, instead of 10 MHz as in FIG. **3**.

FIG. **10** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating delay faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1000** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1014**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1015**, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of 150 MHz are applied to CK**1** **711** to detect or locate delay faults within the clock domain CD**1** **702**. Second, two capture pulses of 100 MHz are applied to CK**2** **714** to detect or locate delay faults within the clock domain CD**2** **703**. Third, two capture pulses of 100 MHz are applied to CK**3** **717** to detect or locate delay faults within the clock domain CD**3** **704**. Fourth, two capture pulses of 66 MHz are applied to CK**4** **720** to detect or locate delay faults within the clock domain CD**4** **705**.

In addition, the stuck-at faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1008** between the rising edge of the second capture pulse of CK**1** **711** and the rising edge of the first capture pulse of CK**2** **714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCD**1** **706**.

The same principle applies to the relative clock delay **1010** between CK**2** **714** and CK**3** **717**, and the relative clock delay **1012** between CK**3** **717** and CK**4** **720** for capturing the output responses, **727** and **731**, through CCD**2** **707** and CCD**3** **708**, respectively.

The daisy-chain clock-triggering technique is used to generate and order the sequence of capture clocks one after the other in the following way: The rising edge of the last pulse in the shift cycle triggers the event **1001** of applying 0 to the global scan enable GSE **801**, switching the test operation from the shift cycle to the capture cycle. The falling edge of GSE **801** triggers the event **1002** of applying two capture pulses to CK**1** **711**. Similarly, the rising edge of the second capture pulse of CK**1** **711** triggers the event **1003** of applying two capture pulses to CK**2** **714**, the rising edge of the second capture pulse of CK**2** **714** triggers the event **1004** of applying two capture pulses to CK**3** **717**, and the rising edge of the second capture pulse of CK**3** **717** triggers the event **1005** of applying two capture pulses to CK**4** **720**. Finally, the rising edge of the second capture pulse of CK**4** **720** triggers the event **1006** of applying 1 to the global scan enable GSE **801**, switching the test operation from the capture cycle to the shift cycle. This daisy-chain clock-triggering technique is also used to order the sequence of capture clocks in FIG. **9** and FIGS. **11** to **20**.

FIG. **11** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating delay faults within each clock domain and stuck-at faults crossing clock domains with a shortened yet ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1100** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1108**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1109**, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of frequency 150 MHz are applied to CK**1** **711** and two clock pulses of frequency 100 MHz are applied to CK**3** **717**, simultaneously, to detect or locate delay faults within the clock domain CD**1** **702** and CD**3** **704**, respectively. Second, two capture pulses of frequency 100 MHz are applied to CK**2** **714** and two capture pulses of frequency 66 MHz are applied to CK**4** **720**, simultaneously, to detect or locate delay faults within the clock domain CD**2** **703** and CD**4** **705**, respectively.

In addition, the stuck-at faults which can be reached from lines **721**, **728**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition

is satisfied: The relative clock delay **1102** between the rising edge of the second capture pulse of CK**1** **711** and the rising edge of the first capture pulse of CK**2** **714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCD**1** **706**.

The same principle applies to the relative clock delay **1104** between CK**3** **717** and CK**2** **714**, and the relative clock delay **1106** between CK**3** **717** and CK**4** **720** for capturing the output responses, **726** and **731**, through CCD**2** **707** and CCD**3** **708**, respectively.

FIG. **12** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and delay faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1200** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1204**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1205**, 4 sets of capture clock pulses are applied in the following order: First, one capture pulse of 150 MHz is applied to CK**1** **711** to detect or locate stuck-at faults within the clock domain CD**1** **702**. Second, one capture pulse of 100 MHz is applied to CK**2** **714** to detect or locate stuck-at faults within the clock domain CD**2** **703**. Third, one capture pulse of 100 MHz is applied to CK**3** **717** to detect or locate stuck-at faults within the clock domain CD**3** **704**. Fourth, one capture pulse of 66MHz is applied to CK**4** **720** to detect or locate stuck-at faults within the clock domain CD**4** **705**.

In addition, the delay faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delays **1201** between the rising edge of the capture pulse of CK**1** **711** and the rising edge of the capture pulse of CK**2** **714** must be adjusted to meet the at-speed timing requirements for paths from **721** to **723**. Similarly, the relative clock delay **1202** between CK**2** **714** and CK**3** **717**, and the relative clock delay **1203** between CK**3** **717** and CK**4** **720**, must be adjusted to meet the at-speed timing requirements for paths from **725** to **727**, and paths from **729** to **731**, respectively.

FIG. **13** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating delay faults within each clock domain and delay faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1300** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1308**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1309**, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of 150 MHz are applied to CK**1** **711** to detect or locate delay faults within the clock domain CD**1** **702**. Second, two capture pulses of 100 MHz are applied to CK**2** **714** to detect or locate delay faults within the clock domain CD**2** **703**.

Third, two capture pulses of 100 MHz are applied to CK**3** **717** to detect or locate delay faults within the clock domain CD**3** **704**. Fourth, two capture pulses of 66 MHz are applied to CK**4** **720** to detect or locate delay faults within the clock domain CD**4** **705**.

In addition, the delay faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1302** between the rising edge of the second capture pulse of CK**1** **711** and the rising edge of the first capture pulse of CK**2** **714** must be adjusted to meet the at-speed timing requirements for paths from **721** to **723**. Similarly, the relative clock delay **1304** between CK**2** **714** and CK**3** **717**, and the relative clock delay **1306** between CK**3** **717** and CK**4** **720**, must be adjusted to meet the at-speed timing requirements for paths from **725** to **727**, and paths from **729** and **731**, respectively.

FIG. **14** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating delay faults within each clock domain and stuck-at faults crossing clock domains with a reordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1400** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1408**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1409**, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of 66 MHz are applied to CK**4** **720** to detect or locate delay faults within the clock domain CD**4** **705**. Second, two capture pulses of 100 MHz are applied to CK**3** **717** to detect or locate delay faults within the clock domain CD**3** **704**. Third, two capture pulses of 100 MHz are applied to CK**2** **714** to detect or locate delay faults within the clock domain CD**2** **703**. Fourth, two capture pulses of 150 MHz are applied to CK**1** **711** to detect or locate delay faults within the clock domain CD**1** **702**.

In addition, the stuck-at faults which can be reached from lines **724**, **728**, and **732** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1402** between the rising edge of the second capture pulse of CK**4** **720** and the rising edge of the first capture pulse of CK**3** **717** must be adjusted so that no races or timing violations would occur while the output responses **730** are captured through the crossing clock-domain logic block CCD**3** **708**.

The same principle applies to the relative clock delay **1404** between CK**3** **717** and CK**2** **714**, and the relative clock delay **1406** between CK**2** **714** and CK**1** **711** for capturing output responses, **726** and **722**, through CCD**2** **707** and CCD**1** **706**, respectively

FIG. **15** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating additional delay faults within each clock domain and additional stuck-at faults crossing clock domains with an expanded yet ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1500** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1514**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66

MHz, are applied through capture clocks, CK1 711 to CK4 720, to shift stimuli to all scan cells within all clock domains, CD1 702 to CD4 705.

During each capture cycle 1515, seven sets of double-capture pulses are applied in the following order: First, two capture pulses of 150 MHz are applied to CK1 711. Second, two capture pulses of 100 MHz are applied to CK2 714. Third, two capture pulses of 100 MHz are applied to CK3 717. Fourth, two capture pulses of 66 MHz are applied to CK4 720. Fifth, two capture pulses of 100 MHz are applied to CK3 717. Sixth, two capture pulses of 100 MHz are applied to CK2 714. Seventh, two capture pulses of 150 MHz are applied to CK1 711.

For the capture clock CK1 711, the second pulse and the third pulse are used to launch the transition needed for detecting or locating delay faults within the clock domain CD1 702. Since the transition is generated by two close-to-functional patterns, the risk of activating a false path is lower. In addition, additional delay faults within the clock domain CD1 702 can be detected or located by the transition. The same results also apply to the clock domains CD2 703 and CD3 704.

In addition, the stuck-at faults which can be reached from lines 724, 728, and 732 in the crossing clock-domain logic blocks CCD1 706 to CCD3 708, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay 1508 between the rising edge of the second capture pulse of CK4 720 and the rising edge of the first capture pulse of CK3 717 must be adjusted so that no races or timing violations would occur while the output responses 730 are captured through the crossing clock-domain logic block CCD3 708.

The same principle applies to the relative clock delay 1510 between CK3 717 and CK2 714, and the relative clock delay 1512 between CK2 714 and CK1 711 for capturing output responses, 726 and 722, through CCD2 707 and CCD1 706, respectively.

FIG. 16 shows a timing diagram of a full-scan design given in FIG. 7, of one embodiment of the invention for detecting or locating 2-cycle delay faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that some paths in the clock domains, CD1 702 to CD4 705, need two cycles for signals to pass through. The timing diagram 1600 shows the sequence of waveforms of the 4 capture clocks, CK1 711 to CK4 720, operating at different frequencies.

During each shift cycle 1608, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK1 711 to CK4 720, to shift stimuli to all scan cells within all clock domains, CD1 702 to CD4 705.

During each capture cycle 1609, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of 75 MHz (half of 150 MHz) are applied to CK1 711 to detect or locate 2-cycle delay faults within the clock domain CD1 702. Second, two capture pulses of 50 MHz (half of 100 MHz) are applied to CK2 714 to detect or locate 2-cycle delay faults within the clock domain CD2 703. Third, two capture pulses of 50 MHz (half of 100 MHz) are applied to CK3 717 to detect or locate 2-cycle delay faults within the clock domain CD3 704. Fourth, two capture pulses of 33 MHz (half of 66 MHz) are applied to CK4 720 to detect or locate 2-cycle delay faults within the clock domain CD4 705.

In addition, the stuck-at faults which can be reached from lines 721, 725, and 729 in the crossing clock-domain logic blocks CCD1 706 to CCD3 708, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay 1602 between the rising edge of the second capture pulse of CK1 711 and the rising edge of the first capture pulse of CK2 714 must be adjusted so that no races or timing violations would occur while the output responses 723 are captured through the crossing clock-domain logic block CCD1 706.

The same principle applies to the relative clock delay 1604 between CK2 714 and CK3 717, and the relative clock delay 1606 between CK3 717 and CK4 720 for capturing output responses, 727 and 731, through CCD2 707 and CCD3 708, respectively.

FIG. 17 shows a timing diagram of a full-scan design given in FIG. 7, of one embodiment of the invention for detecting or locating 2-cycle delay faults within each clock domain and 2-cycle delay faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that some paths in the clock domains, CD1 702 to CD4 705, and the crossing clock-domain logic blocks, CCD1 706 to CCD3 708, need two cycles for signals to pass through. The timing diagram 1700 shows the sequence of waveforms of the 4 capture clocks, CK1 711 to CK4 720, operating at different frequencies.

During each shift cycle 1708, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK1 711 to CK4 720, to shift stimuli to all scan cells within all clock domains, CD1 702 to CD4 705.

During each capture cycle 1709, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of 75 MHz (half of 150 MHz) are applied to CK1 711 to detect or locate 2-cycle delay faults within the clock domain CD1 702. Second, two capture pulses of 50 MHz (half of 100 MHz) are applied to CK2 714 to detect or locate 2-cycle delay faults within the clock domain CD2 703. Third, two capture pulses of 50 MHz (half of 100 MHz) are applied to CK3 717 to detect or locate 2-cycle delay faults within the clock domain CD3 704. Fourth, two capture pulses of 33 MHz (half of 66 MHz) are applied to CK4 720 to detect or locate 2-cycle delay faults within the clock domain CD4 705.

In addition, the 2-cycle delay faults which can be reached from lines 721, 725, and 729 in the crossing clock-domain logic blocks CCD1 706 to CCD3 708, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay 1702 between the rising edge of the second capture pulse of CK1 711 and the rising edge of the first capture pulse of CK2 714 must be adjusted to meet the 2-cycle timing requirements for paths from 721 to 723. Similarly, the relative clock delay 1704 between CK2 714 and CK3 717, and the relative clock delay 1706 between CK3 717 and CK4 720, must be adjusted to meet the 2-cycle timing requirements for paths from 725 to 727, and paths from 729 and 731, respectively.

FIG. 18 shows a timing diagram of a feed-forward partial-scan design given in FIG. 7, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that the clock domains CD1 702 to CD4 705 contain a number of un-scanned storage cells that form a sequential depth of no more than 2. The timing diagram 1800 shows the sequence of waveforms of the 4 capture clocks, CK1 711 to CK4 720, operating at different frequencies.

During each shift cycle 1812, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK1 711 to CK4 720, to shift stimuli to all scan cells within all clock domains, CD1 702 to CD4 705.

During each capture cycle **1813**, 4 sets of capture clock pulses are applied in the following order: First, three pulses of 150 MHz, two being functional pulses and one being a capture pulse, are applied to CK**1** **711** to detect or locate stuck-at faults within the clock domain CD**1** **702**. Second, three pulses of 100 MHz, two being functional pulses and one being a capture pulse, are applied to CK**2** **714** to detect or locate stuck-at faults within the clock domain CD**2** **703**. Third, three pulses of 100 MHz, two being functional pulses and one being a capture pulse, are applied to CK**3** **717** to detect or locate stuck-at faults within the clock domain CD**3** **704**. Fourth, three pulses of frequency 66 MHz, two being functional pulses and one being a capture pulse, are applied to CK**4** **717** to detect or locate stuck-at faults within the clock domain CD**4** **705**.

In addition, the stuck-at faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1803** between the rising edge of the second capture pulse of CK**1** **711** and the rising edge of the first capture pulse of CK**2** **714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCD**1** **706**.

The same principle applies to the relative clock delay **1806** between CK**2** **714** and CK**3** **717**, and the relative clock delay **1809** between CK**3** **717** and CK**4** **720** for capturing output responses, **727** and **731**, through CCD**2** **707** and CCD**3** **708**, respectively.

FIG. **19** shows a timing diagram of a feed-forward partial-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating delay faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that the clock domains CD**1** **702** to CD**4** **705** contain a number of un-scanned storage cells that form a sequential depth of no more than 2. The timing diagram **1900** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1916**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1917**, 4 sets of capture clock pulses are applied in the following order: First, 4 pulses of 150 MHz, two being functional pulses and two being capture pulses, are applied to CK**1** **711** to detect or locate delay faults within the clock domain CD**1** **702**. Second, 4 pulses of 100 MHz, two being functional pulses and two being capture pulses, are applied to CK**2** **714** to detect or locate delay faults within the clock domain CD**2** **703**. Third, 4 pulses of 100 MHz, two being functional pulses and two being capture pulses, are applied to CK**3** **717** to detect or locate delay faults within the clock domain CD**3** **704**. Fourth, 4 pulses of 66 MHz, two being functional pulses and two being capture pulses, are applied to CK**4** **720** to detect or locate delay faults within the clock domain CD**4** **705**.

In addition, the stuck-at faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1904** between the rising edge of the second capture pulse of CK**1** **711** and the rising edge of the first capture pulse of CK**2** **714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCD**1** **706**.

The same principle applies to the relative clock delay **1908** between CK**2** **714** and CK**3** **717**, and the relative clock delay **1912** between CK**3** **717** and CK**4** **720** for capturing output responses, **727** and **731**, through CCD**2** **707** and CCD**3** **708**, respectively.

FIG. **20** shows a timing diagram of a feed-forward partial-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating 2-cycle delay faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that the clock domains CD**1** **702** to CD**4** **705** contain a number of un-scanned storage cells that form a sequential depth of no more than 2. Also, it is assumed that some paths in the clock domains, CD**1** **702** to CD**4** **705**, need two cycles for signals to pass through. The timing diagram **2000** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **2016**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **2017**, 4 sets of capture clock pulses are applied in the following order: First, 4 pulses, two being functional pulses of 150 MHz and two being capture pulses of 75 MHz (half of 150 MHz), are applied to CK**1** **711** to detect or locate 2-cycle delay faults within the clock domain CD**1** **702**. Second, 4 pulses, two being functional pulses of 100 MHz and two being capture pulses of 50 MHz (half of 100 MHz), are applied to CK**2** **714** to detect or locate 2-cycle delay faults within the clock domain CD**2** **703**. Third, 4 pulses, two being functional pulses of 100 MHz and two being capture pulses of 50 MHz (half of 100 MHz), are applied to CK**3** **717** to detect or locate 2-cycle delay faults within the clock domain CD**3** **704**. Fourth, 4 pulses, 2 being functional pulses of 66 MHz and 2 being capture pulses of 33 MHz (half of 66 MHz), are applied to CK**4** **720** to detect or locate 2-cycle delay faults within the clock domain CD**4** **705**.

In addition, the stuck-at faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **2004** between the rising edge of the second capture pulse of CK**1** **711** and the rising edge of the first capture pulse of CK**2** **714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCDI **706**.

The same principle applies to the relative clock delay **2008** between CK**2** **714** and CK**3** **717**, and the relative clock delay **2012** between CK**3** **717** and CK**4** **720** for capturing output responses, **727** and **731**, through CCD**2** **707** and CCD**3** **708**, respectively.

FIG. **21** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where the capture clock CK**2** during the capture cycle is chosen to diagnose faults captured by CK**2** in self-test or scan-test mode.

Fault diagnosis is the procedure by which a fault is located. In order to achieve this goal, it is often necessary to use an approach where a test pattern detects only portion of faults while guaranteeing no other faults are detected. If the test pattern does produce a response that matches the observed response, it can then be declared that the portion must contain

at least one actual fault. Then the same approach to the portion of the faults to further localize the actual faults.

The timing diagram **2100** shows a way to facilitate this approach. In the capture cycle **2107**, two capture pulses of 100 MHz are only applied to the capture clock CK**2** **714** while the other three capture clocks are held inactive. As a result, for delay faults, only those in the clock domain CD**2** **703** are detected. In addition, for stuck-at faults, only those in the crossing clock-domain logic blocks CCD**1** **706** and CCD**2** **707** and the clock domain CD**2** **703** are detected. Obviously, this clock timing helps in fault diagnosis.

FIG. **22** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where the capture clocks CK**1** and CK**3** during the capture cycle are chosen to diagnose faults captured by CK**1** and CK**3** in self-test or scan-test mode.

The diagram **2200** shows one more timing scheme that can help fault diagnosis as described in the description of FIG. **21**. In the capture cycle **2208**, two capture pulses of 150 MHz are applied to the capture clock CK**1** **711** and two capture pulses of 100 MHz are applied to the capture clock CK**3** **717** while the other two capture clocks are held inactive. As a result, for delay faults, only those in the clock domain CD**1** **702** and CD**3** **704** are detected. In addition, for stuck-at faults, only those in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708** and the clock domains CD**1** **702** and CD**3** **703** are detected. Obviously, this clock timing helps in fault diagnosis.

FIG. **23** shows a timing diagram of the full-scan design given in FIG. **1**, in accordance with the present invention, where all capture clocks during the shift cycle are skewed to reduce power consumption. The timing diagram **2300** only shows the waveforms for the capture clocks CK**1** **111** to CK**4** **120** during the shift cycle. For the capture cycle, any capture timing control methods claimed in this patent can be applied.

During the shift cycle **2305**, clock pulses for the clocks CK**1** **111** to CK**4** **120** are skewed by properly setting the delay **2301** between the shift pulses for the clocks CK**1** **111** and CK**2** **114**, the delay **2302** between the shift pulses for the clocks CK**2** **114** and CK**3** **117**, the delay **2303** between the shift pulses for the clocks CK**3** **117** and CK**4** **120**, the delay **2304** between the shift pulses for the clocks CK**4** **120** and CK**1** **111**. As a result, both peak power consumption and average power consumption are reduced. In addition, during the capture cycle, the PRPG **212** is driven by clock CK**2** **114**, the first-arrived capture clock, and the MISR **221** is driven by clock CK**3** **117**, the last-arrived capture clock, in the shared PRPG-MISR pair **228** in FIG. **2**. Thus, the ordered capture sequence guarantees the correct capture operation when a shared PRPG-MISR pair is used for a plurality of clock domains in self-test mode.

FIG. **24** shows a flow chart of one embodiment of the invention. The multiple-capture self-test computer-aided design (CAD) system **2400** accepts the user-supplied HDL code or netlist **2402** together with the self-test control files **2401** and the chosen foundry library **2403**. The self-test control files **2401** contain all set-up information and scripts required for compilation **2404**, self-test rule check **2406**, self-test rule repair **2507**, and multiple-capture self-test synthesis **2408**. As a result, an equivalent combinational circuit model **2409** is generated. Then, combinational fault simulation **2410** can be performed. Finally, post-processing **2411** is used to produce the final self-test HDL code or netlist **2412** as well as the HDL test benches and ATE test programs **2413**. All reports and errors are saved in the report files **2414**.

The multiple-capture self-test synthesis **2408** uses a hierarchical approach in which it synthesizes a plurality of PRPG-MISR pairs one at a time for each individual clock domain or combined clock domains, then synthesizes a central self-test controller which includes an error indicator, and finally stitches the central self-test controller together with synthesized PRPG-MISR pairs. Each PRPG-MISR pair is composed of a PRPG, an optional phase shifter, an optional space compactor, a MISR, and a comparator. In addition, during PRPG-MISR synthesis, a number of spare scan cells can be inserted into selected clock domains. As a result, the central self-test controller can remain intact even when the need for circuit modification rises at a later stage.

FIG. **25** shows a flow chart of one embodiment of the invention. The multiple-capture scan-test computer-aided design (CAD) system **2500** accepts the user-supplied HDL code or netlist **2502** together with the scan control files **2501** and the chosen foundry library **2503**. The scan control files **2501** contain all set-up information and scripts required for compilation **2504**, scan rule check **2506**, scan rule repair **2507**, and multiple-capture scan synthesis **2508**. As a result, an equivalent combinational circuit model **2509** is generated. Then, combinational ATPG **2510** can be performed. Finally, post-processing **2511** is used to produce the final scan HDL netlist **2512** as well as the HDL test benches and ATE test programs **2513**. All reports and errors are saved in the report files **2514**.

Having thus described presently preferred embodiments of the present invention, it can now be appreciated that the objectives of the invention have been fully achieved. And it will be understood by those skilled in the art that many changes in construction & circuitry, and widely differing embodiments & applications of the invention will suggest themselves without departing from the spirit and scope of the present invention. The disclosures and the description herein are intended to be illustrative and are not in any sense limitation of the invention, more preferably defined in the scope of the invention by the Claims appended hereto and their equivalents.

What is claimed is:

1. A computer-aided design (CAD) method for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in scan-test and self-test mode, where N>1, each clock domain having one capture clock and a plurality of scan cells, each capture clock comprising a selected number of shift clock pulses and a selected number of capture clock pulses, each shift clock pulse comprising a clock pulse applied in scan mode, each capture clock pulse comprising a clock pulse applied in normal mode, said CAD method comprising the computer-implemented steps of:

(a) compiling the HDL code or netlist that represents said integrated circuit or circuit assembly in physical form into a design database;

(b) performing test rule check for checking whether said design database contains any multiple-capture rule violations in said scan-test or said self-test mode;

(c) performing test rule repair until all said multiple-capture rule violations have been fixed;

(d) performing multiple-capture test synthesis for generating a testable HDL code or netlist; and

(e) generating HDL test benches and automatic test equipment (ATE) test programs for verifying the correctness of said testable HDL netlist in said scan-test or said self-test mode.

2. The CAD method of claim **1**, wherein said steps of (a)-(e) accept user-supplied scan control information and report the results and errors, if any.

3. The CAD method of claim 1, wherein said performing test rule check further comprises determining the number of clock domains and capture clocks required for scan-test, the clock domains to be tested concurrently, the ordered sequence of capture clocks to be applied for scan-test, and the capture clocks to be operated at the rated clock speeds or at selected clock speeds.

4. The CAD method of claim 1, wherein said performing multiple-capture test synthesis further comprises inserting spare scan cells into selected clock domains.

5. The CAD method of claim 1, wherein said performing multiple-capture test synthesis further comprises implementing the method of:

(f) generating and shifting-in N test stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during a shift-in operation;

(g) applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least a plurality of capture clock pulses from two or more selected capture clocks placed in a sequential order such that all clock domains are never triggered simultaneously during a capture operation; and

(h) shifting-out said N output responses for analysis with said expected output responses, during a shift-out operation.

6. The CAD method of claim 1, wherein said generating HDL test benches and ATE test programs further comprises the steps of transforming said design database into an equivalent combinational circuit model based on said ordered sequence of capture clocks, performing combinational automatic test pattern generation (ATPG) to generate the circuit's test patterns, and performing fault simulation to report its fault coverage.

7. The CAD method of claim 1, wherein said generating HDL test benches and ATE test programs further comprises performing combinational logic simulation on said combinational circuit model to compute said circuit's signatures when a compact operation is employed to compact said circuit's output responses.

* * * * *

US007779323B2

(12) **United States Patent**
Wang et al.

(10) **Patent No.: US 7,779,323 B2**
(45) **Date of Patent: *Aug. 17, 2010**

(54) **MULTIPLE-CAPTURE DFT SYSTEM FOR DETECTING OR LOCATING CROSSING CLOCK-DOMAIN FAULTS DURING SELF-TEST OR SCAN-TEST**

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(73) Assignee: **Syntest Technologies, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **12/222,931**

(22) Filed: **Aug. 20, 2008**

(65) **Prior Publication Data**

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Related U.S. Application Data

(60) Continuation of application No. 11/806,098, filed on May 30, 2007, now Pat. No. 7,434,126, which is a division of application No. 11/098,703, filed on Apr. 5, 2005, now Pat. No. 7,260,756, which is a division of application No. 10/067,372, filed on Feb. 7, 2002, now Pat. No. 7,007,213.

(60) Provisional application No. 60/268,601, filed on Feb. 15, 2001.

(51) **Int. Cl.**
G01R 31/28 (2006.01)
G06F 11/00 (2006.01)

(52) **U.S. Cl.** **714/731**; 714/744; 714/732

(58) **Field of Classification Search** 714/724, 714/726, 731, 732, 744, 741
See application file for complete search history.

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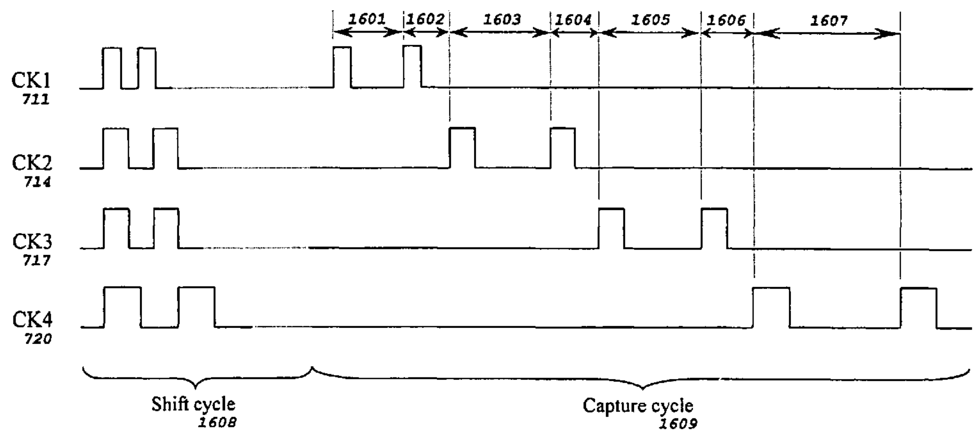
(Continued)

Primary Examiner—Cynthia Britt
(74) *Attorney, Agent, or Firm*—Bacon & Thomas, PLLC

(57) **ABSTRACT**

A method and apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in self-test or scan-test mode, where N>1 and each domain has a plurality of scan cells. The method and apparatus allows generating and loading N pseudorandom or predetermined stimuli to all the scan cells within the N clock domains in the integrated circuit or circuit assembly during the shift operation, applying an ordered sequence of capture clocks to all the scan cells within the N clock domains during the capture operation, compacting or comparing N output responses of all the scan cells for analysis during the compact/compare operation, and repeating the above process until a predetermined limiting criteria is reached. A computer-aided design (CAD) system is further developed to realize the method and synthesize the apparatus.

21 Claims, 25 Drawing Sheets



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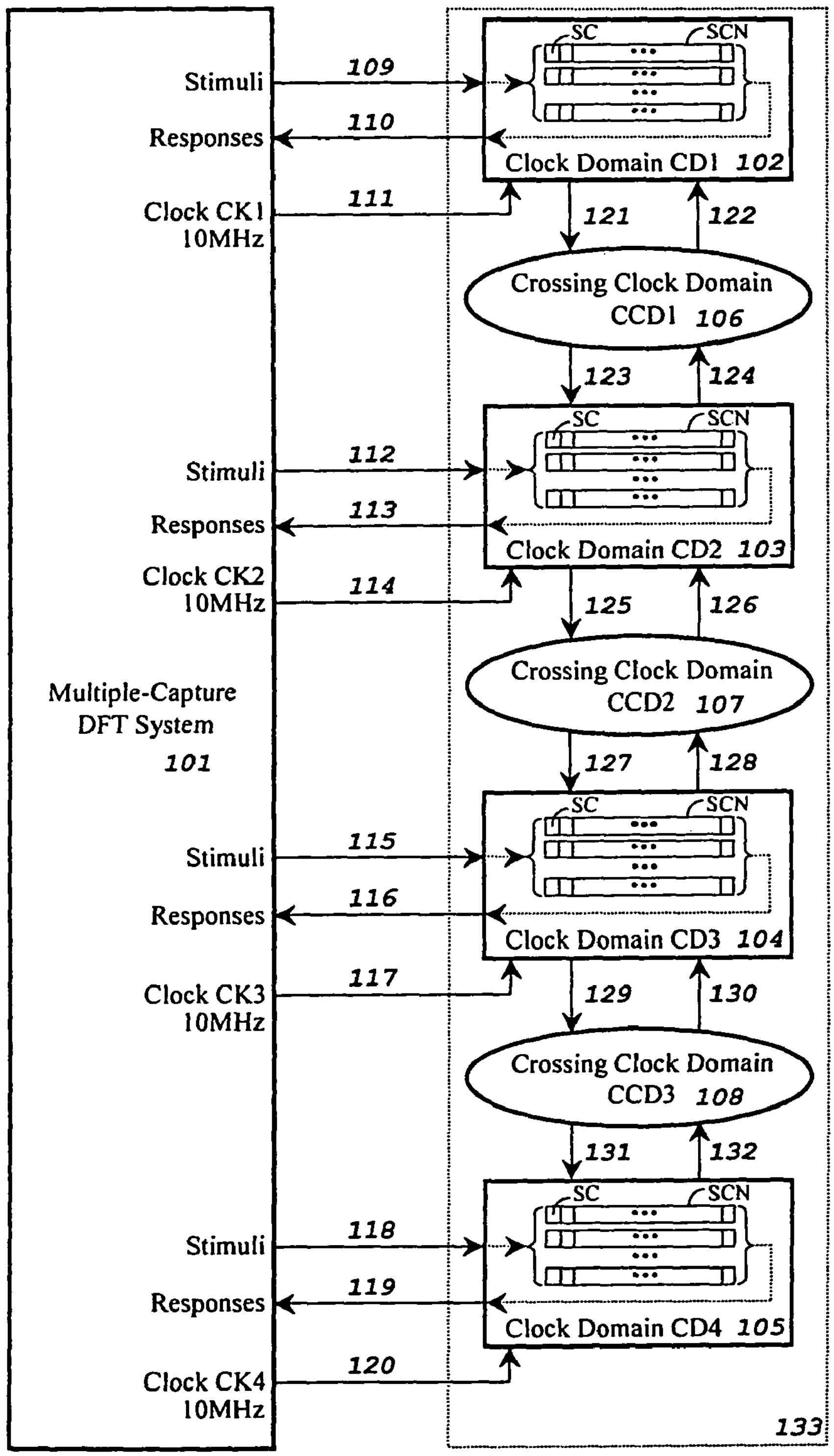
Multiple-Capture
DFT System
101
Stimuli
Responses
Clock CK1
10MHz
Clock CK2
10MHz
Clock CK3
10MHz
Clock CK4
10MHz
109
110
111
112
113
114
115
116
117
118
119
120
SC
SCN
Clock Domain CD1 102
Clock Domain CD2 103
Clock Domain CD3 104
Clock Domain CD4 105
Crossing Clock Domain
CCD1 106
Crossing Clock Domain
CCD2 107
Crossing Clock Domain
CCD3 108
121
122
123
124
125
126
127
128
129
130
131
132
133

FIG. 1

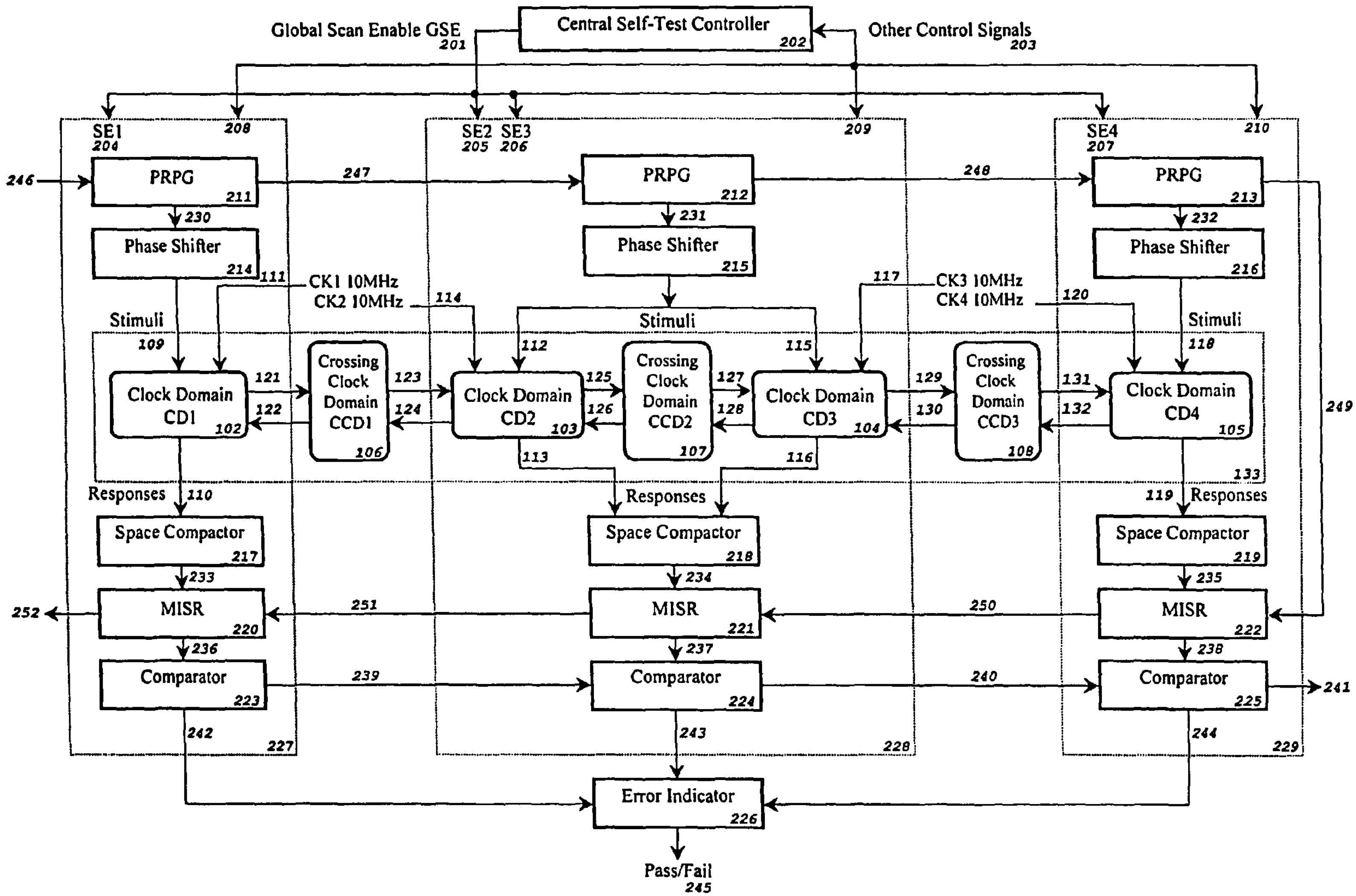
Central Self-Test Controller 202
Global Scan Enable GSE 201
Other Control Signals 203
SE1 204
SE2 205
SE3 206
SE4 207
208
209
210
246
PRPG 211
PRPG 212
PRPG 213
247
248
230
231
232
Phase Shifter 214
Phase Shifter 215
Phase Shifter 216
111
CK1 10MHz
CK2 10MHz
114
117
CK3 10MHz
CK4 10MHz
120
Stimuli 109
Stimuli
Stimuli 118
112
115
Clock Domain CD1 102
Crossing Clock Domain CCD1 106
Clock Domain CD2 103
Crossing Clock Domain CCD2 107
Clock Domain CD3 104
Crossing Clock Domain CCD3 108
Clock Domain CD4 105
121
122
123
124
125
126
127
128
129
130
131
132
113
116
133
249
Responses 110
Responses
119 Responses
Space Compactor 217
Space Compactor 218
Space Compactor 219
233
234
235
MISR 220
MISR 221
MISR 222
252
251
250
236
237
238
Comparator 223
Comparator 224
Comparator 225
239
240
241
242
243
244
227
228
229
Error Indicator 226
Pass/Fail 245

FIG. 2

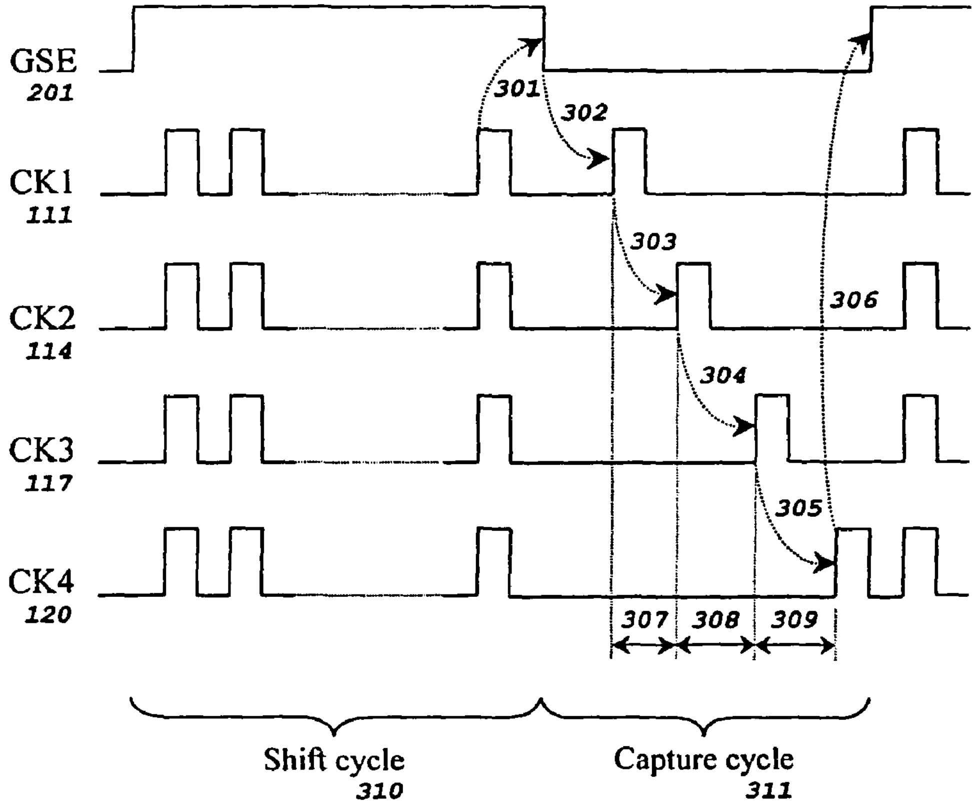
GSE
201
CK1
111
CK2
114
CK3
117
CK4
120
301
302
303
304
305
306
307
308
309
Shift cycle
310
Capture cycle
311

FIG. 3

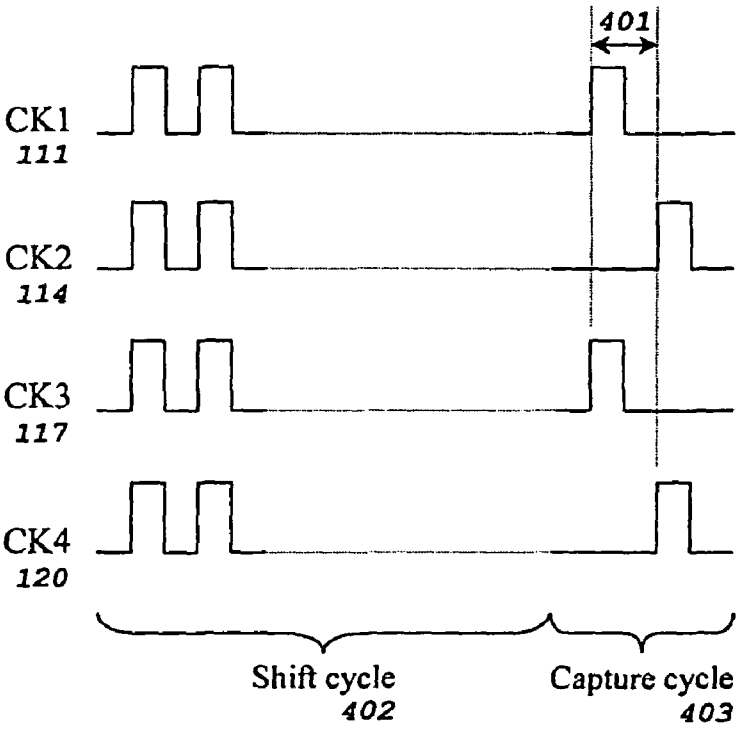
401
CK1
111
CK2
114
CK3
117
CK4
120
Shift cycle
402
Capture cycle
403

FIG. 4

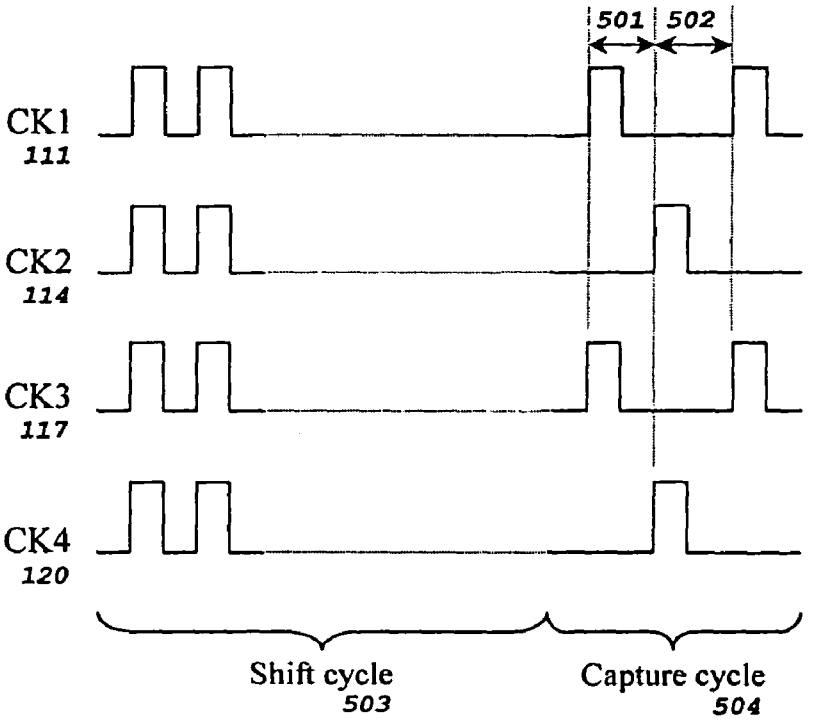
501
502
CK1
111
CK2
114
CK3
117
CK4
120
Shift cycle
503
Capture cycle
504

FIG. 5

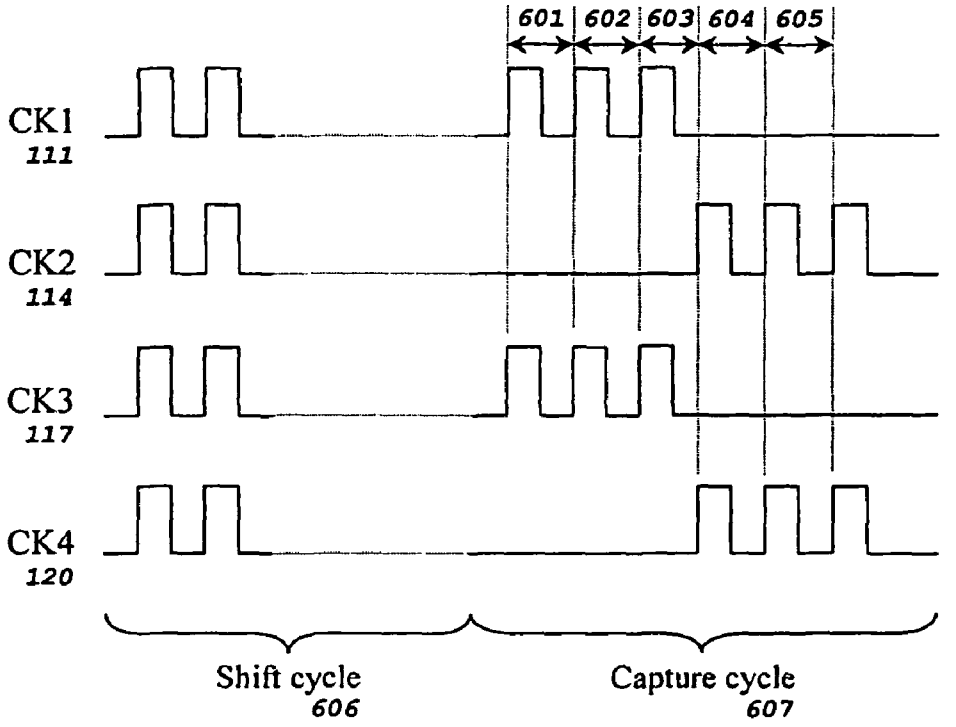
601
602
603
604
605
CK1
111
CK2
114
CK3
117
CK4
120
Shift cycle
606
Capture cycle
607

FIG. 6

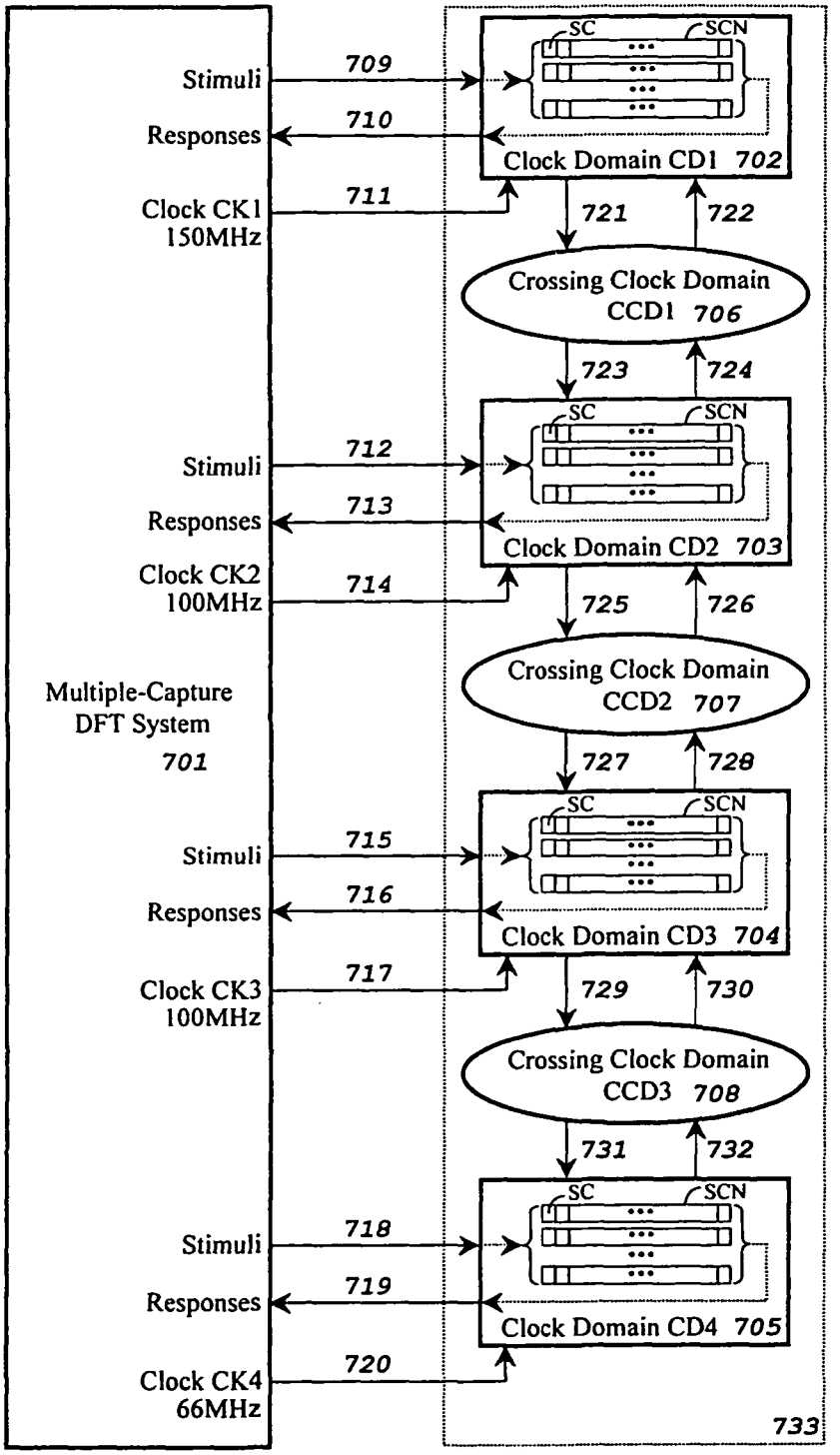
Stimuli
709
Responses
710
Clock CK1
150MHz
711
SC
SCN
Clock Domain CD1 702
721
722
Crossing Clock Domain
CCD1 706
723
724
Stimuli
712
Responses
713
Clock CK2
100MHz
714
Clock Domain CD2 703
725
726
Crossing Clock Domain
CCD2 707
727
728
Multiple-Capture
DFT System
701
Stimuli
715
Responses
716
Clock CK3
100MHz
717
Clock Domain CD3 704
729
730
Crossing Clock Domain
CCD3 708
731
732
Stimuli
718
Responses
719
Clock CK4
66MHz
720
Clock Domain CD4 705
733

FIG. 7

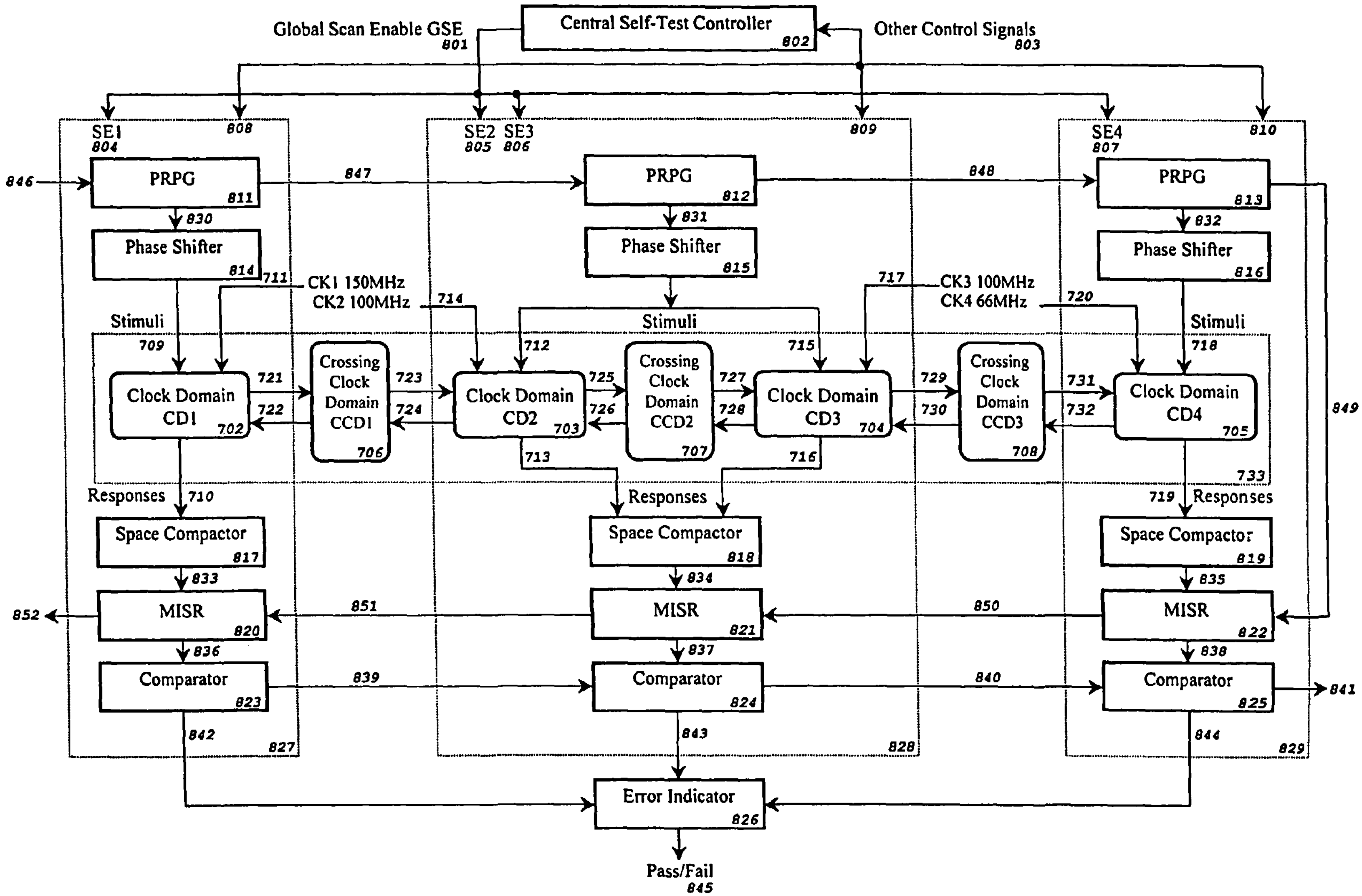
Central Self-Test Controller
802
Global Scan Enable GSE
801
Other Control Signals
803
SE1
804
808
SE2
805
SE3
806
809
SE4
807
810
846
PRPG
811
847
PRPG
812
848
PRPG
813
830
831
832
Phase Shifter
814
Phase Shifter
815
Phase Shifter
816
711
CK1 150MHz
CK2 100MHz
714
717
CK3 100MHz
CK4 66MHz
720
Stimuli
709
Stimuli
712
715
Stimuli
718
Clock Domain
CD1
702
721
722
Crossing
Clock
Domain
CCD1
706
723
724
Clock Domain
CD2
703
725
726
Crossing
Clock
Domain
CCD2
707
727
728
Clock Domain
CD3
704
729
730
Crossing
Clock
Domain
CCD3
708
731
732
Clock Domain
CD4
705
849
733
Responses
710
713
716
Responses
719
Responses
Space Compactor
817
Space Compactor
818
Space Compactor
819
833
834
835
852
MISR
820
851
MISR
821
850
MISR
822
836
837
838
Comparator
823
839
Comparator
824
840
Comparator
825
841
842
827
843
828
844
829
Error Indicator
826
Pass/Fail
845

FIG. 8

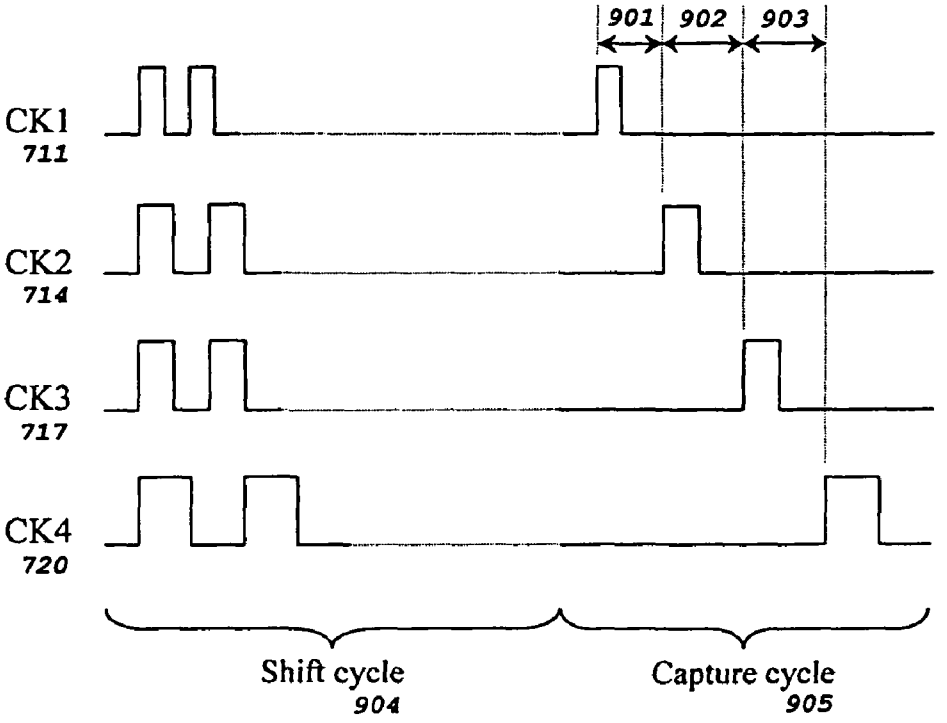
901
902
903
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
904
Capture cycle
905

FIG. 9

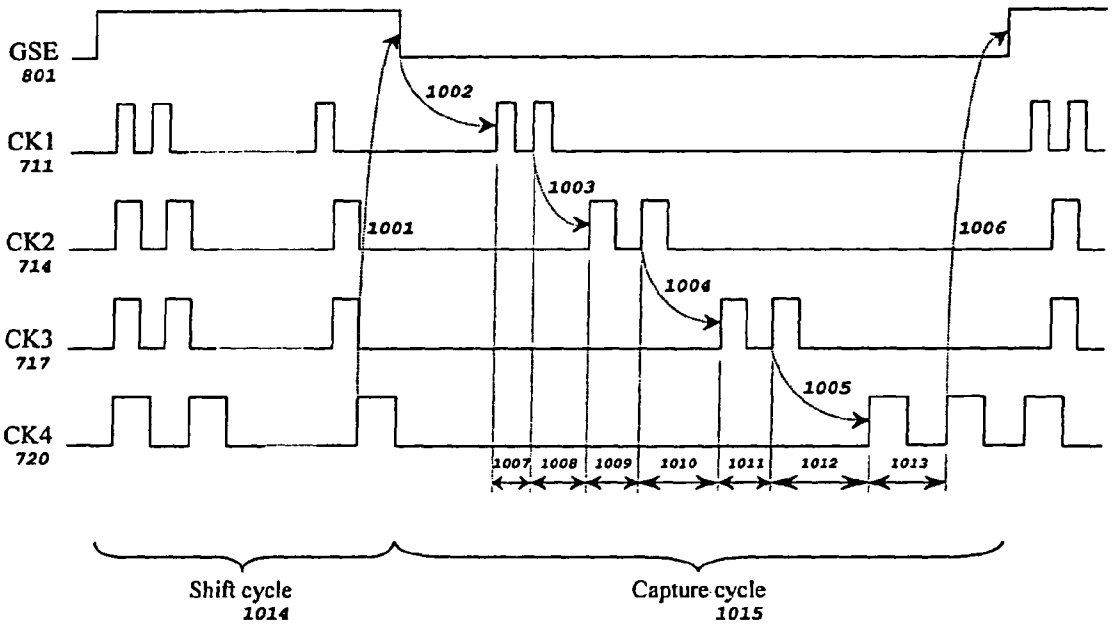
GSE
801
CK1
711
CK2
714
CK3
717
CK4
720
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
Shift cycle
1014
Capture cycle
1015

FIG. 10

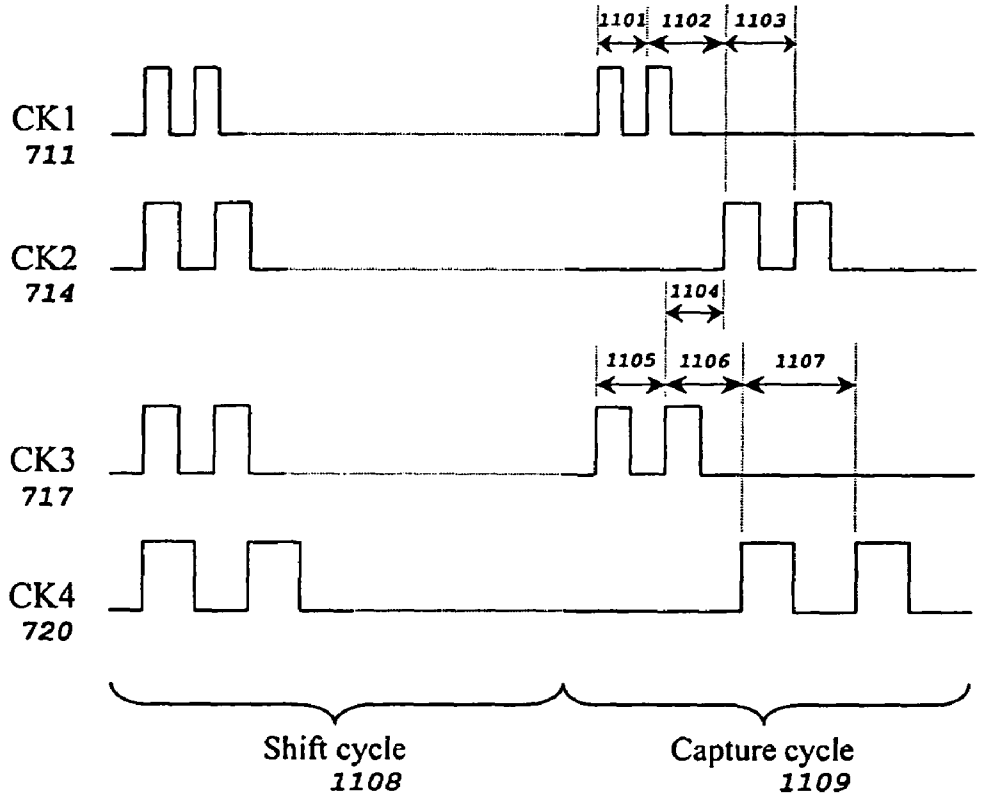
1101
1102
1103
CK1
711
CK2
714
1104
1105
1106
1107
CK3
717
CK4
720
Shift cycle
1108
Capture cycle
1109

FIG. 11

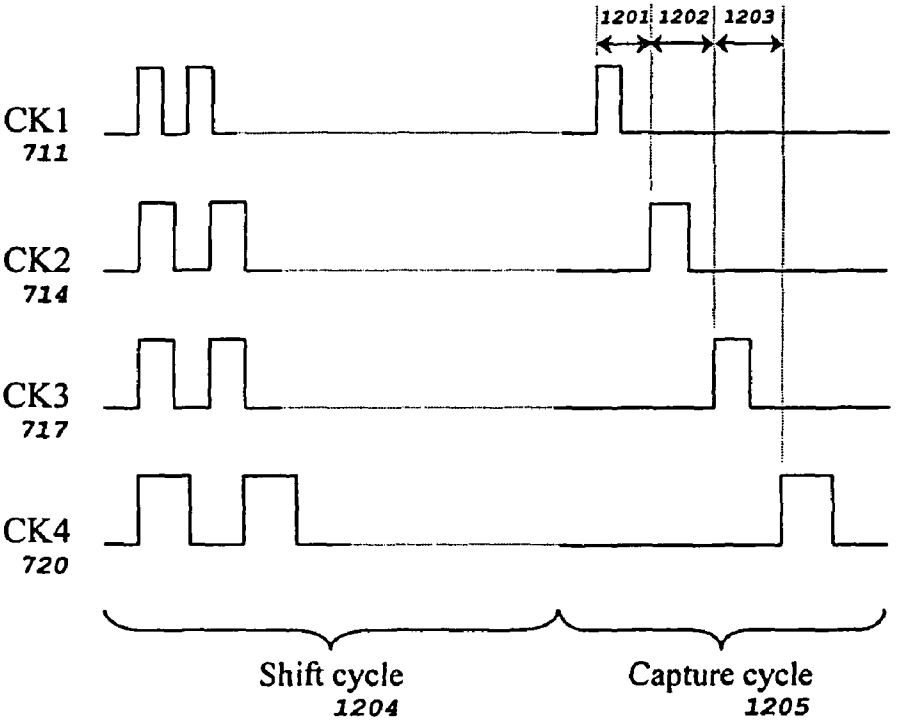
1201
1202
1203
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1204
Capture cycle
1205

FIG. 12

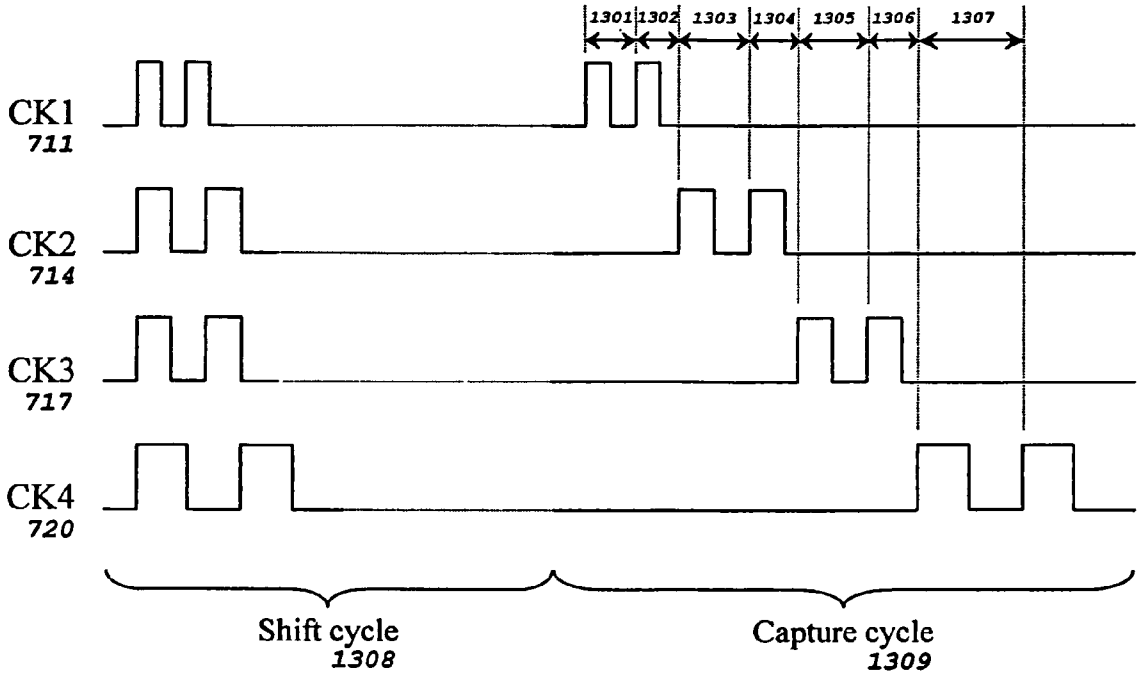
1301
1302
1303
1304
1305
1306
1307
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1308
Capture cycle
1309

FIG. 13

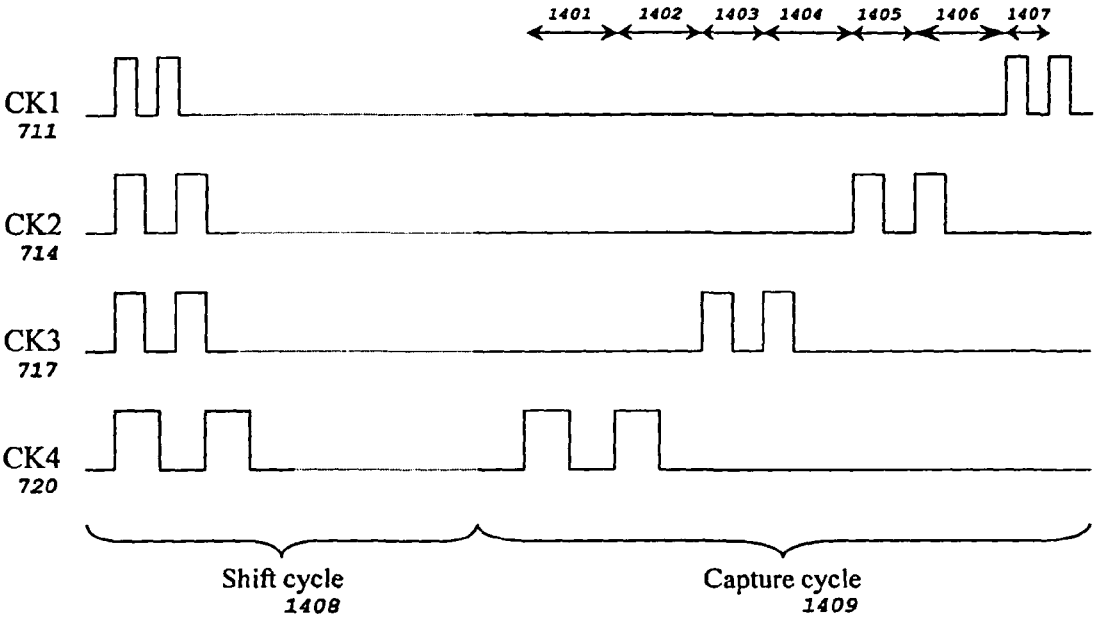
1401
1402
1403
1404
1405
1406
1407
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1408
Capture cycle
1409

FIG. 14

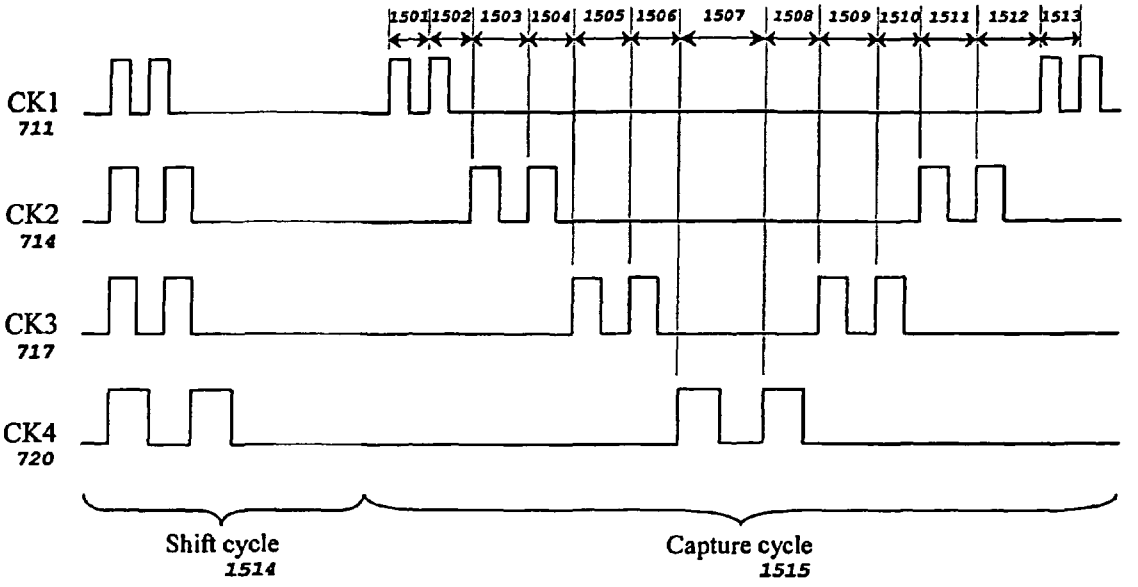
1501 1502 1503 1504 1505 1506 1507 1508 1509 1510 1511 1512 1513
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1514
Capture cycle
1515

FIG. 15

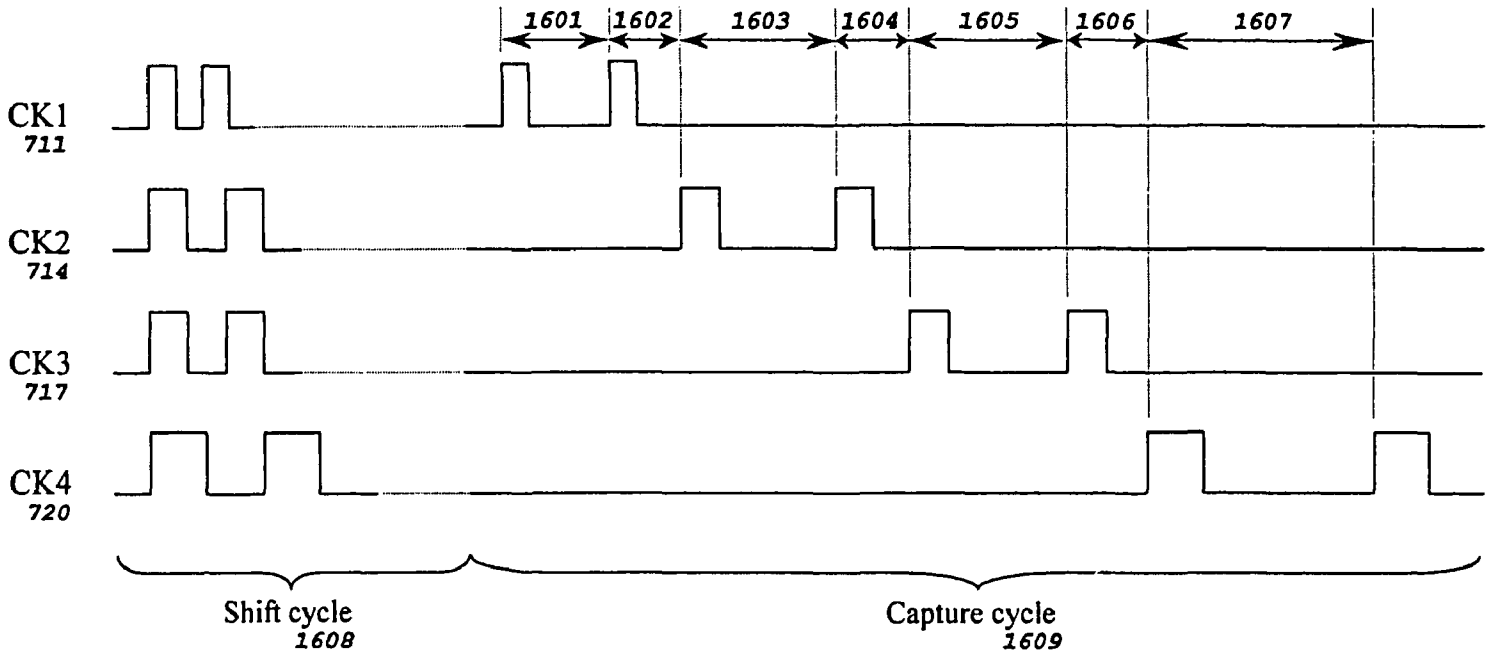
1601
1602
1603
1604
1605
1606
1607
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1608
Capture cycle
1609

FIG. 16

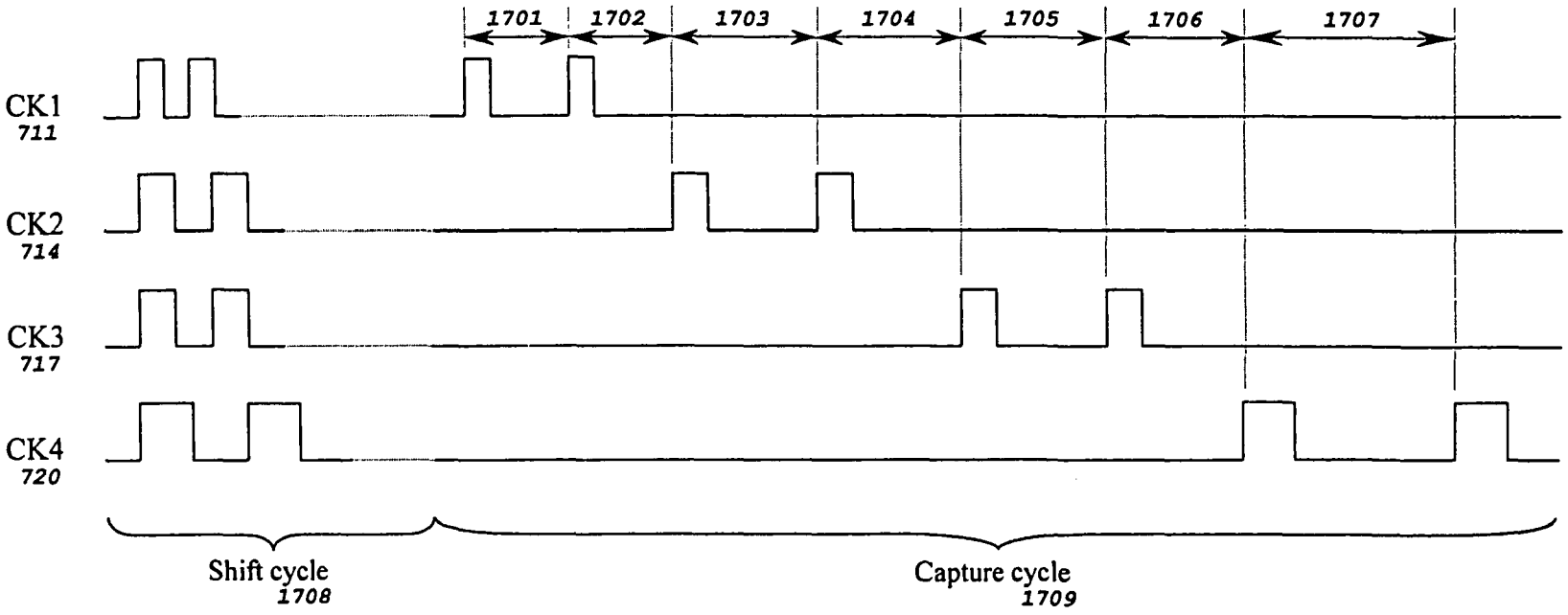
1701
1702
1703
1704
1705
1706
1707
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1708
Capture cycle
1709

FIG. 17

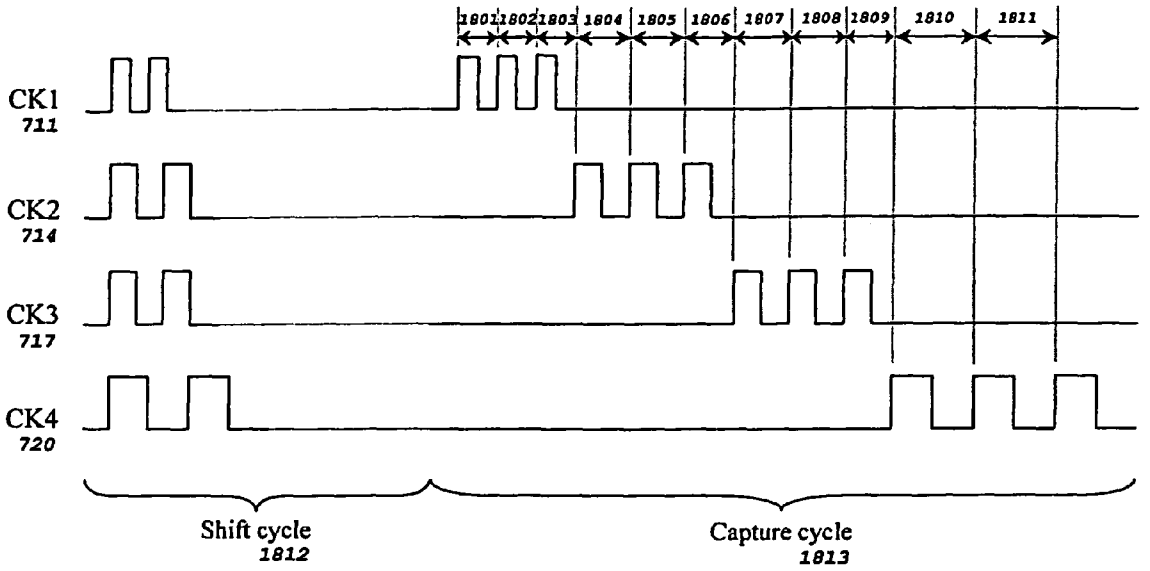
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1812
Capture cycle
1813

FIG. 18

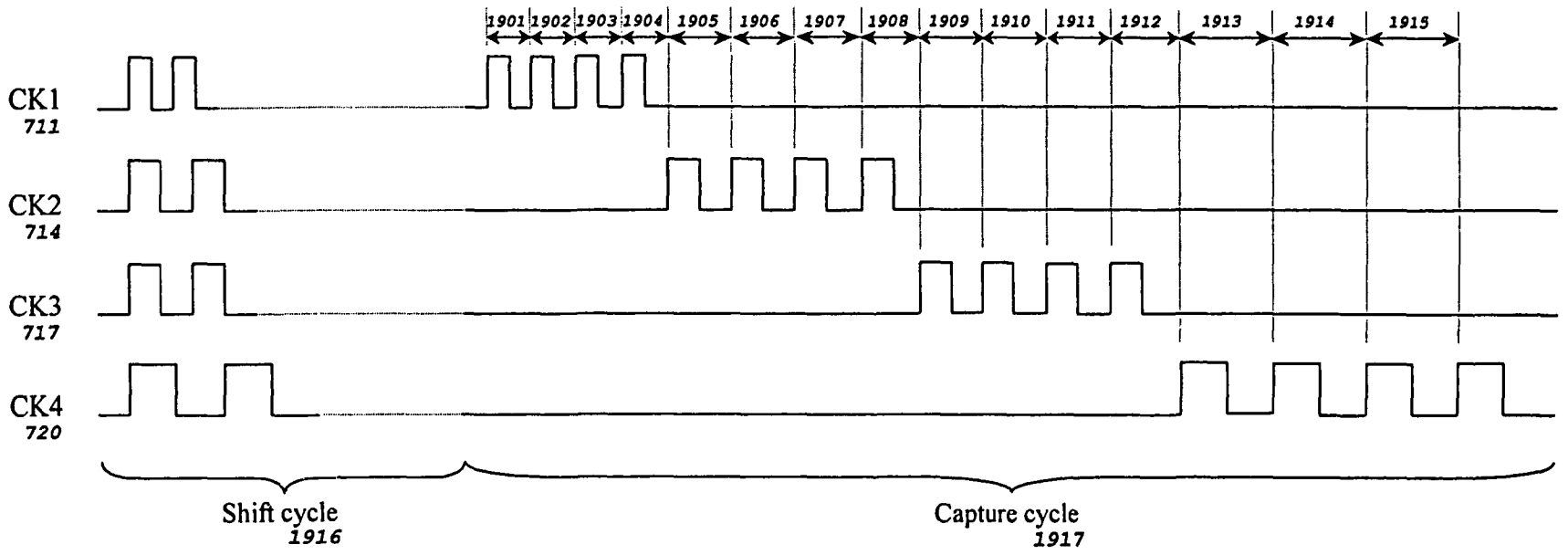
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
CK1
711
CK2
714
CK3
717
CK4
720
Shift cycle
1916
Capture cycle
1917

FIG. 19

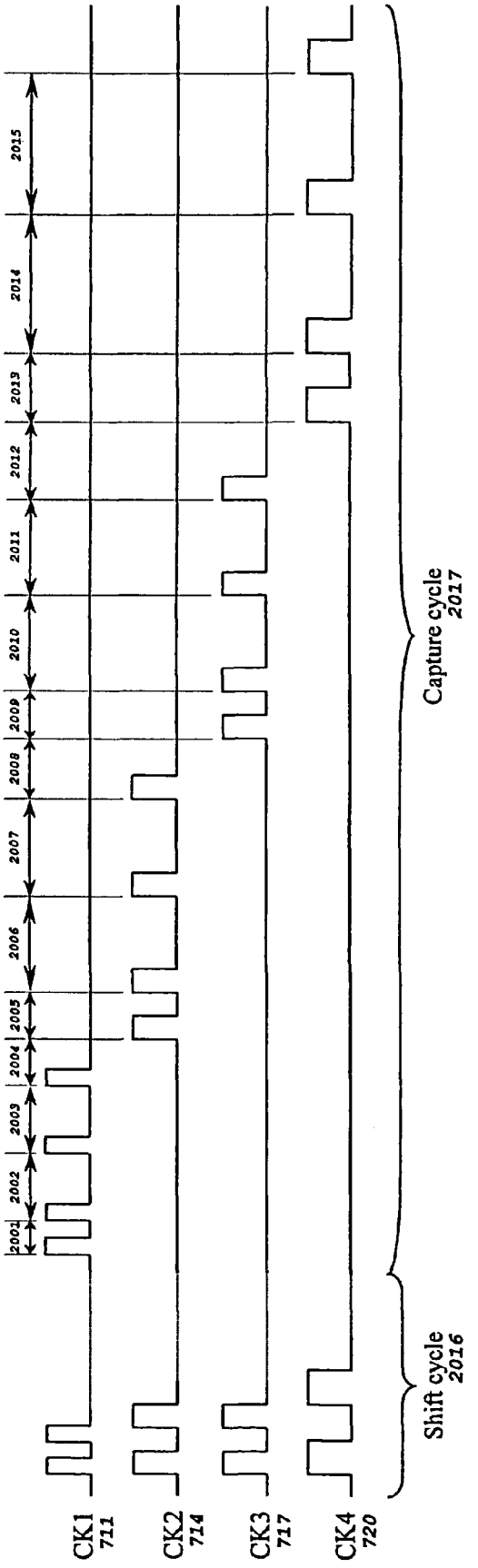
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
Capture cycle 2017
Shift cycle 2016
CK1 711
CK2 714
CK3 717
CK4 720

FIG. 20

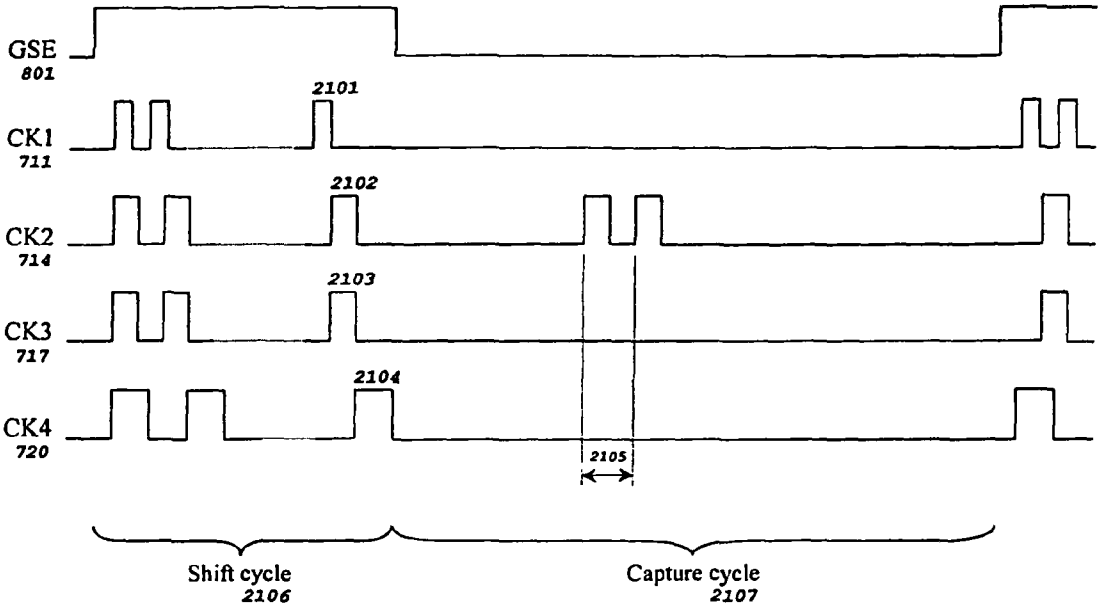
GSE
801
2101
CK1
711
2102
CK2
714
2103
CK3
717
2104
CK4
720
2105
Shift cycle
2106
Capture cycle
2107

FIG. 21

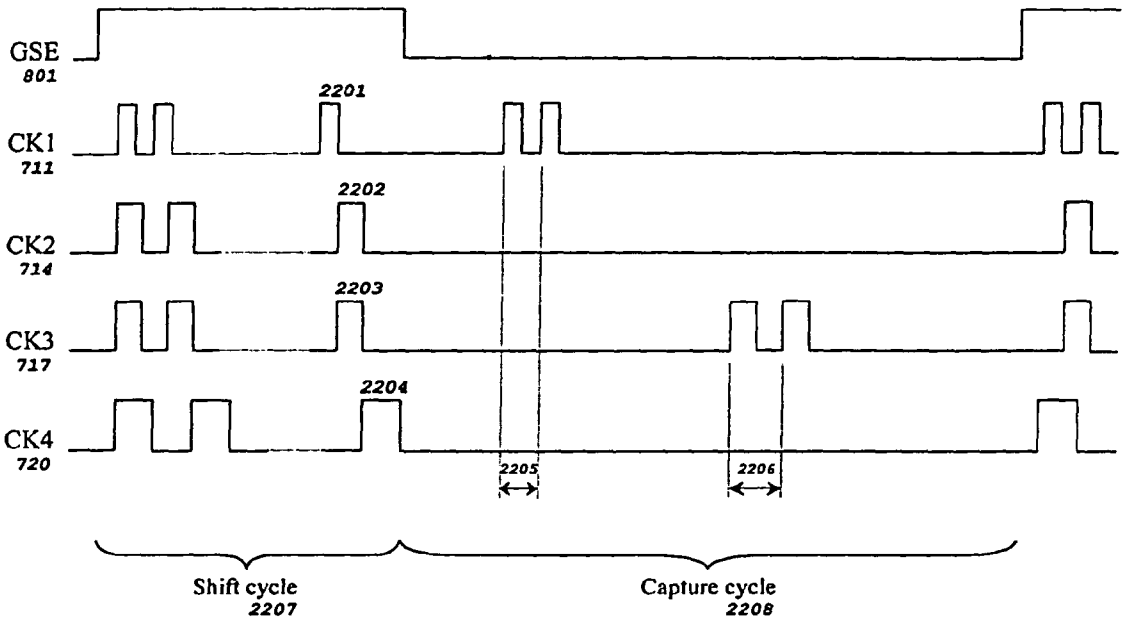
GSE
801
2201
CK1
711
2202
CK2
714
2203
CK3
717
2204
CK4
720
2205
2206
Shift cycle
2207
Capture cycle
2208

FIG. 22

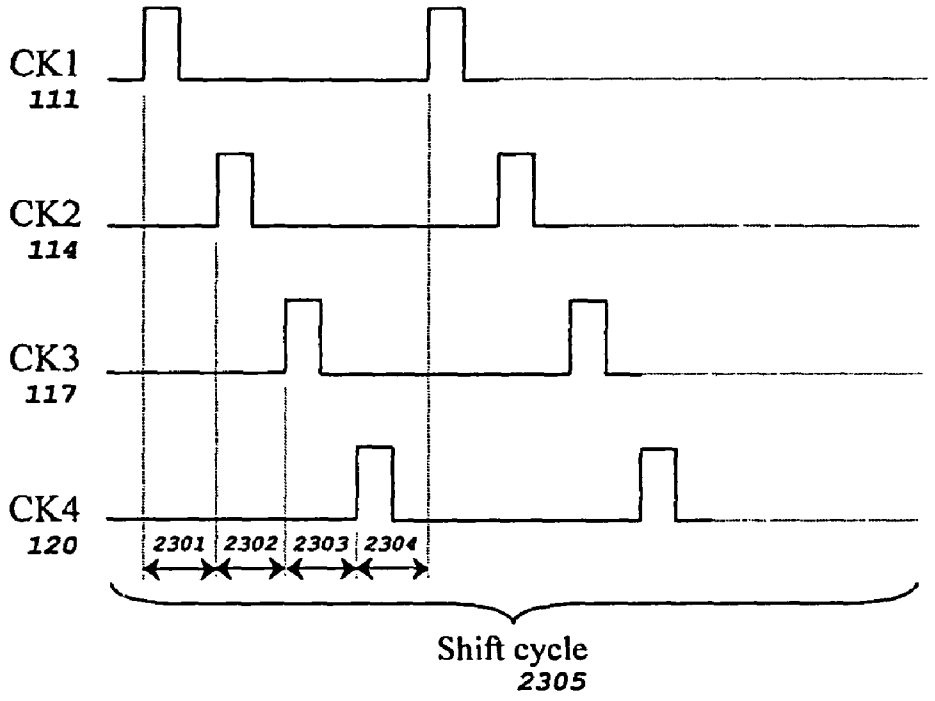
CK1
111
CK2
114
CK3
117
CK4
120
2301
2302
2303
2304
Shift cycle
2305

FIG. 23

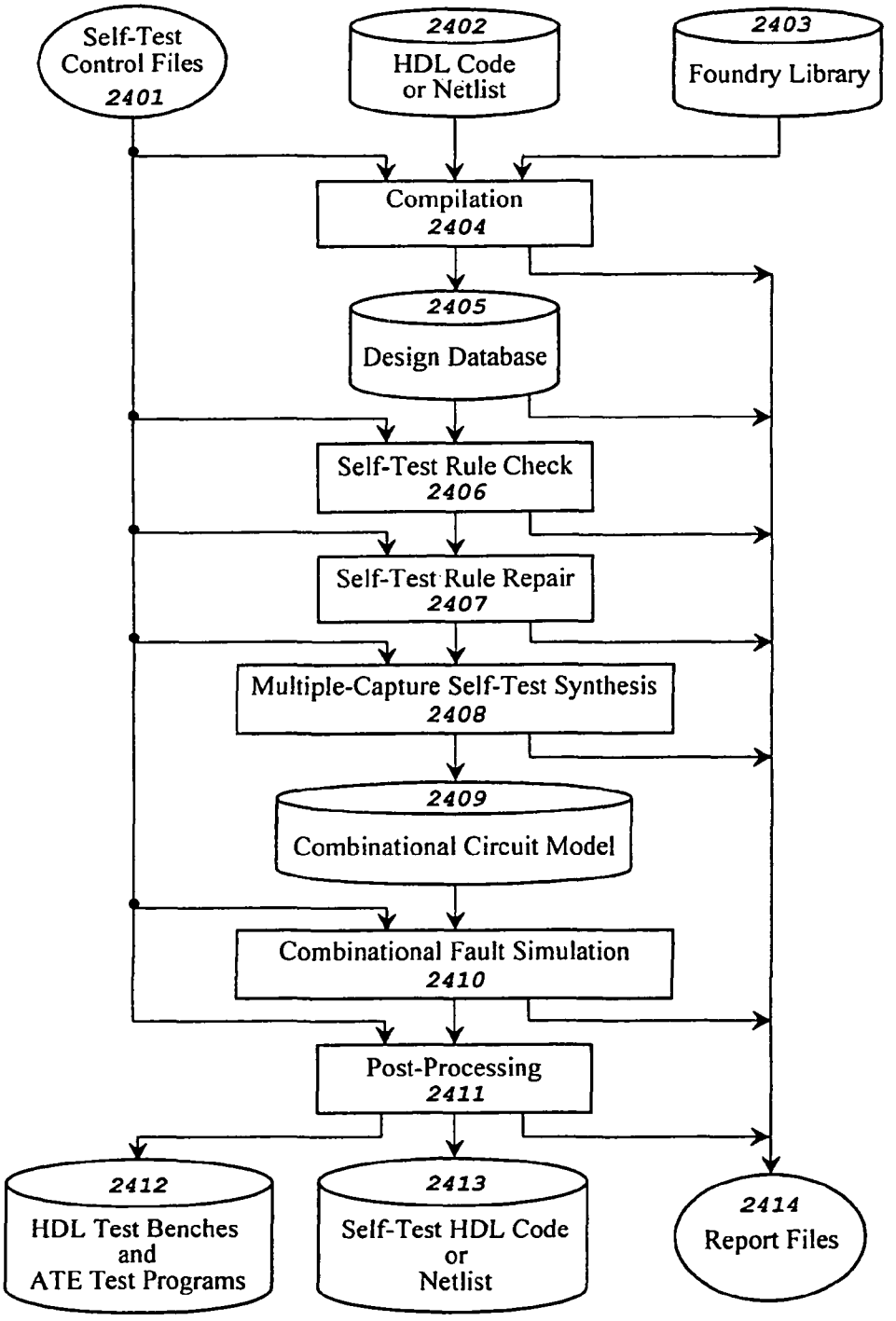
Self-Test Control Files 2401
2402 HDL Code or Netlist
2403 Foundry Library
Compilation 2404
2405 Design Database
Self-Test Rule Check 2406
Self-Test Rule Repair 2407
Multiple-Capture Self-Test Synthesis 2408
2409 Combinational Circuit Model
Combinational Fault Simulation 2410
Post-Processing 2411
2412 HDL Test Benches and ATE Test Programs
2413 Self-Test HDL Code or Netlist
2414 Report Files

FIG. 24

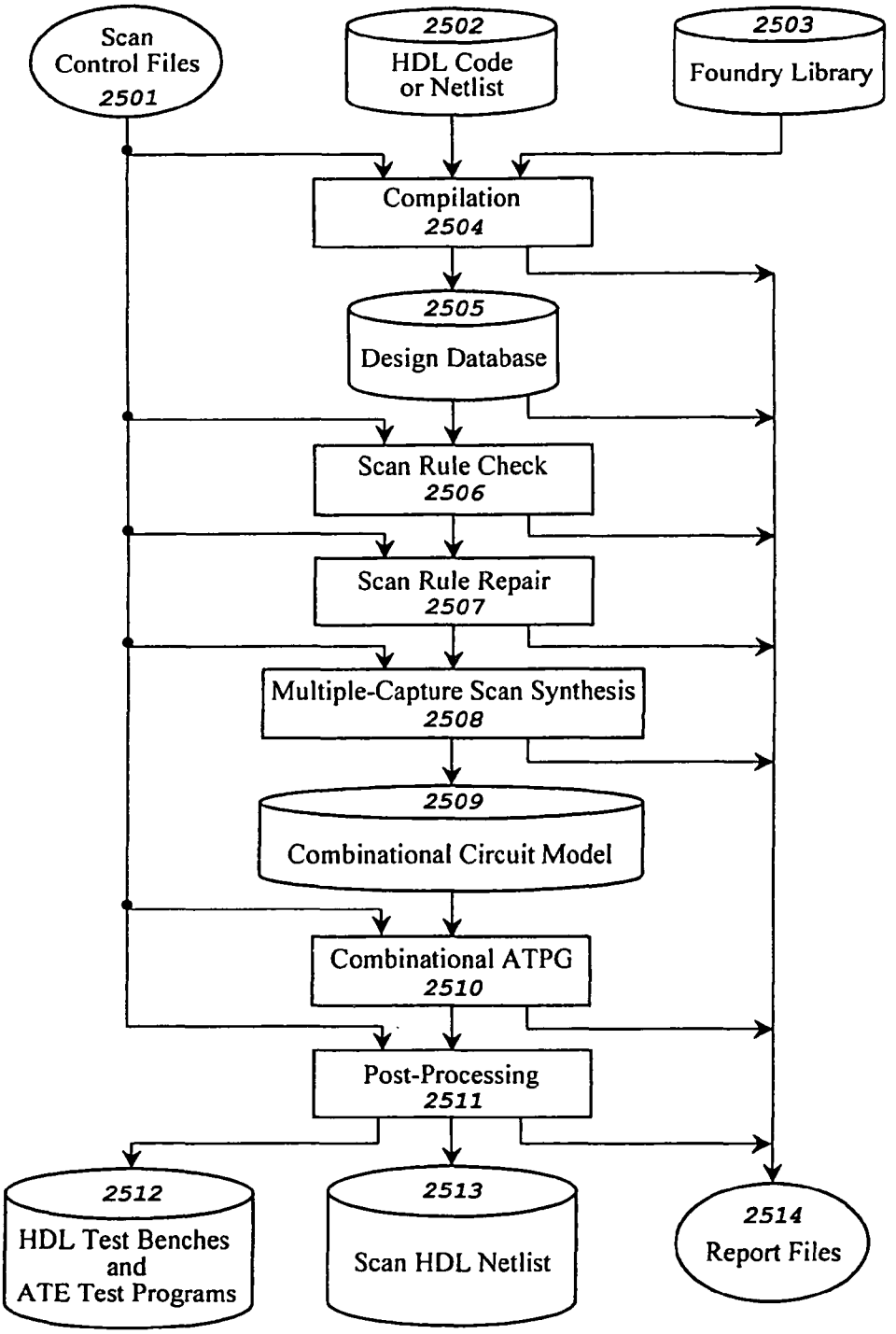
Scan Control Files 2501
2502 HDL Code or Netlist
2503 Foundry Library
Compilation 2504
2505 Design Database
Scan Rule Check 2506
Scan Rule Repair 2507
Multiple-Capture Scan Synthesis 2508
2509 Combinational Circuit Model
Combinational ATPG 2510
Post-Processing 2511
2512 HDL Test Benches and ATE Test Programs
2513 Scan HDL Netlist
2514 Report Files

FIG. 25

MULTIPLE-CAPTURE DFT SYSTEM FOR DETECTING OR LOCATING CROSSING CLOCK-DOMAIN FAULTS DURING SELF-TEST OR SCAN-TEST

RELATED APPLICATION DATA

The present application is a continuation application of application Ser. No. 11/806,098, filed May 30, 2007 now U.S. Pat. No. 7,434,126 and now allowed, which is a divisional application of application Ser. No. 11/098,703 filed Apr. 5, 2005, now U.S. Pat. No. 7,260,756, which in turn is a divisional application of Ser. No. 10/067,372 filed Feb. 7, 2002, now U.S. Pat. No. 7,007,213, which claims the benefit of provisional application No. 60/268,601 filed Feb. 15, 2001 which is hereby incorporated by reference, and for which priority is claimed for all of the above.

TECHNICAL FIELD

The present invention generally relates to the testing of logic designs in an integrated circuit or circuit assembly embedded with design-for-test (DFT) techniques. Specifically, the present invention relates to the detection or location of logic faults within each clock domain and logic faults crossing any two clock domains, during self-test or scan-test, in an integrated circuit or circuit assembly.

BACKGROUND OF THE INVENTION

In this specification, the term integrated circuit is used to describe a chip or MCM (multi-chip module) embedded with design-for-test (DFT) techniques. The terms circuit assembly and printed circuit board will be considered interchangeable. The term circuit assembly includes printed circuit boards as well as other types of circuit assemblies. A circuit assembly is a combination of integrated circuits. The resulting combination is manufactured to form a physical or functional unit.

An integrated circuit or circuit assembly, in general, contains two or more systems clocks, each controlling one module or logic block, called clock domain. Each system clock is either directly coming from a primary input (edge pin/connector) or generated internally. These system clocks can operate at totally unrelated frequencies (clock speeds), at submultiples of each other, at the same frequency but with different clock skews, or at a mix of the above. Due to clock skews among these system clocks, when a DFT technique, such as self-test or scan-test, is employed, it is very likely that faults associated with the function between two clock domains, called crossing clock-domain faults, will become difficult to test. In the worst case, these crossing clock-domain faults when propagating into the receiving clock domain could completely block detection or location of all faults within that clock domain. Thus, in order to solve the fault propagation problem, DFT approaches are proposed to take over control of all system clocks and reconfigure them as capture clocks.

Prior-art DFT approaches in this area to testing crossing clock-domain faults as well as faults within each clock domain centered on using the isolated DFT, ratio'ed DFT, and one-hot DFT techniques. They are all referred to as single-capture DFT techniques, because none of them can provide multiple skewed capture clocks (or an ordered sequence of capture clocks) in each capture cycle during self-test or scan-test.

In using the isolated DFT technique, all boundary signals crossing a clock domain and flowing into the receiving clock domains are completely blocked or disabled by forcing each of them to a predetermined logic value of 0 or 1. See U.S. Pat. No. 6,327,684 issued to Nadeau-Dostie et al. (2001). This approach, in general, can allow all clock domains to be tested in parallel. The major drawbacks of this approach are that it requires insertion of capture-disabled logic in between clock domains and all scan enable signals each associated with one clock domain must be operated at-speed. The design change could take significant efforts and it might impact normal mode operation. Running all scan enable signals at-speed requires routing them as clock signals using layout clock-tree synthesis (CTS). In addition, since boundary signals can traverse through two clock domains in both directions, this approach requires testing crossing clock-domain faults in two or more test sessions. This could substantially increase the test time required and might make the capture-disabled logic even more complex to implement than anticipated.

In using the ratio'ed DFT technique, all clock domains must be operated at sub-multiples of one reference clock. For instance, assume that a design contains 3 clock domains running at 150 MHz, 80 MHz, and 45 MHz, respectively. The 3 clock domains may have to be operated at 150 MHz, 75 MHz, and 37.5 MHz during testing. See U.S. Pat. No. 5,349,587 issued to Nadeau-Dostie et al. (1994). This approach reduces the complexity of testing a multiple-frequency design and avoids potential races or timing violations crossing clock domains. It can also allow testing of all clock domains in parallel. However, due to changes in clock-domain operating frequencies, this approach loses its self-test or scan-test intent of testing multiple-frequency designs at their rated clock speeds (at-speed) and may require significant design and layout efforts on re-timing (or synchronizing) all clock domains. Power consumption could be also another serious problem because all scan cells (memory elements) are triggered simultaneously every few cycles.

In using the one-shot DFT technique, each crossing clock-domain signal flowing into its receiving clock domains must be initialized to or held at a predetermined logic value of 0 or 1 first. This initialization is usually accomplished by shifting in predetermined logic values to all clock domains so that all crossing clock-domain signals are forced to a known state. Testing is then conducted domain-by-domain, thus, called one-hot testing. See U.S. Pat. No. 5,680,543 issued to Bhawmik et al. (1997). The major benefits of using this approach are that it can still detect or locate crossing clock-domain faults and does not need insertion of disabled logic, in particular, in critical paths crossing clock domains. However, unlike the isolated or ratio'ed DFT approach, this approach requires testing of all clock domains in series, resulting in long test time. It also requires significant design and layout efforts on re-timing (or synchronizing) all clock domains.

Two additional prior-art DFT approaches had also been proposed, one for scan-test, the other for self-test. Both approaches are referred to as multiple-capture DFT techniques, because they can provide multiple skewed capture clocks (or an ordered sequence of capture clocks) in each capture cycle during scan-test or self-test.

The first prior-art multiple-capture DFT approach is to test faults within each clock domain and faults between two clock domains in scan-test mode. See U.S. Pat. No. 6,070,260 issued to Buch et al. (2000) and U.S. Pat. No. 6,195,776 issued to Ruiz et al. (2001). These approaches rest on using multiple skewed scan clocks or multiple skew capture events each operating at the same reduced clock speed in an ATE (automatic test equipment) to detect faults. Combinational ATPG (automatic test pattern generation) is used to generate scan-test patterns and ATE test programs are created to detect

faults in the integrated circuit. Unfortunately, currently available ATPG tools only assume the application of one clock pulse (clock cycle) to each clock domain. Thus, these approaches can only detect stuck-at faults in scan-test mode. No prior art using multiple skewed capture clocks were proposed to test delay or stuck-at faults requiring two or more capture clock pulses for full-scan or partial-scan designs.

The second prior-art multiple-capture DFT approach is to test faults within each clock domain and faults between two clock domains in self-test mode. See the paper co-authored by Hetherington et al. (1999). This approach rests on using multiple shift-followed-by-capture clocks each operating at its operating frequency, in a programmable capture window, to detect faults at-speed. It requires clock suppression, complex scan enable (SE) timing waveforms, and shift clock pulses in the capture window to control the capture operation. These shift clock pulses may also need precise timing alignment. As a result, it becomes quite difficult to perform at-speed self-test for designs containing clock domains operated at totally unrelated frequencies, e.g., 133 MHz and 60 MHz.

Thus, there is a need for an improved method, apparatus, or computer-aided design (CAD) system that allows at-speed or slow-speed testing of faults within clock domains and between any two clock domains using a simple multiple-capture DFT technique. The method and apparatus of the present invention will control the multiple-capture operations of the capture clocks in self-test or scan-test mode. It does not require using shift clock pulses in the capture window, inserting capture-disabled logic in normal mode, applying clock suppression on capture clock pulses, and programming complex timing waveforms on scan enable (SE) signals. In addition, the CAD system of the present invention further comprises the computer-implemented steps of performing multiple-capture self-test or scan synthesis, combinational fault simulation, and combinational ATPG that are currently unavailable in the CAD field using multiple-capture DFT techniques.

SUMMARY OF THE INVENTION

Accordingly, a primary objective of the present invention is to provide an improved multiple-capture DFT system implementing the multiple-capture DFT technique. Such a DFT system will comprise a method or apparatus for allowing at-speed/slow-speed detection or location of faults within all clock domains and faults crossing clock domains in an integrated circuit or circuit assembly. In the present invention, the method or apparatus can be realized and placed inside or external to the integrated circuit or circuit assembly.

A computer-aided design (CAD) system that synthesizes such a DFT system and generates desired HDL test benches and ATE test programs is also included in the present invention. A hardware description language (HDL) is used to represent the integrated circuit includes, but is not limited to, Verilog or VHDL. An ATE is an IC tester or any equipment that realizes the multiple-capture DFT system and is external to the integrated circuit or circuit assembly under test.

The present invention focuses on multiple-capture DFT systems for self-test and scan-test. In a self-test environment, a self-test cycle often comprises 3 major operations: shift, capture, and compact. The shift and compact operations can occur concurrently during each self-test cycle. In order to increase the circuit's fault coverage, it is often necessary to include scan-test cycles to perform top-up ATPG. A scan-test cycle often comprises 3 major operations in a scan-test environment: shift, capture, and compare. The shift and compare operations can occur concurrently during each scan-test cycle. In a mixed self-test and scan-test environment, the scan-test cycle may execute a compact operation rather than the compare operation. Thus, in the present invention, a self-test cycle further comprises the shift, capture, and compare operations, and a scan-test cycle further comprises the shift, capture, and compact operations.

The multiple-capture DFT system of the present invention further comprises any method or apparatus for executing the shift and compact or shift and compare operations concurrently during each self-test or scan-test cycle. It is applicable to test any integrated circuit or circuit assembly which contains N clock domains, where N>1. Each capture clock controls one clock domain and can operate at its rated clock speed (at-speed) or at a reduced clock speed (slow-speed), when desired.

During the shift operation, the multiple-capture DFT system first generates and shifts in (loads) N pseudorandom or predetermined stimuli to all scan cells within all clock domains, concurrently. The shifting frequency is irrelevant to at-speed testing. Depending on needs, a slower frequency can be used to reduce power consumption and a faster frequency can be used to reduce the test application time. The multiple-capture DFT system must wait until all stimuli have been loaded or shifted into all scan cells. By that time, all scan enable (SE) signals each associated with one clock domain shall switch from the shift operation to the capture operation. After the capture operation is completed, all scan enable (SE) signals shall switch from the capture operation to the shift operation. One global scan enable (GSE) signal can be simply used to drive these scan enable signals.

The multiple-capture DFT system of the present invention further comprises any method or apparatus for performing the shift operation at any selected clock speed within each clock domain and using only one global scan enable (GSE) signal to drive all scan enable (SE) signals for at-speed or slow-speed testing. The GSE signal can be also operated at its selected reduced clock speed. Thus, there is no need to route these SE signals as clock signals using layout clock tree synthesis (CTS). This invention applies to any self-test or scan-test method that requires multiple capture clock pulses (without including shift clock pulses) in the capture cycle.

After the shift operation is completed, an ordered sequence of capture clocks is applied to all clock domains. During the capture operation, each ordered sequence contains N capture clocks of which only one or a few will be active at one time. There are no shift clock pulses present within each capture cycle. Testing of delay faults at-speed is now performed by applying two consecutive capture clock pulses (double captures) rather than using the shift-followed-by-capture clock pulses. Performing multiple captures in the capture cycle reduces the risk of delay test invalidation and false paths that might occur due to illegal states in scan cells resulting from filling them with pseudorandom or predetermined stimuli.

In the present invention, the multiple-capture DFT system uses a daisy-chain clock-triggering or token-ring clock-enabling technique to generate and order capture clocks one after the other. One major benefit of using this approach is that the test results are repeatable no matter what clock speed will be used for each capture clock. The problem is it could be difficult to precisely control the relative clock delay between two adjacent capture clocks for testing delay faults between clock domains.

As an example, assume that the capture cycle contains 4 capture clocks, CK**1**, CK**2**, CK**3**, and CK**4**. (Please refer to FIGS. **3** and **10** in the DETAILED DESCRIPTION OF THE DRAWINGS section for further descriptions). The daisy-chain clock-triggering technique implies that completion of

the shift cycle triggers the GSE signal to switch from shift to capture cycle which in turn triggers CK**1**, the rising edge of the last CK**1** pulse triggers CK**2**, the rising edge of the last CK**2** pulse triggers CK**3**, and the rising edge of the last CK**3** pulse triggers CK**4**. Finally, the rising edge of the last CK**4** pulse triggers the GSE signal to switch from capture to shift cycle.

The token-ring clock-enabling technique implies that completion of the shift cycle enables the GSE signal to switch from shift to capture cycle which in turn enables CK**1**, completion of CK**1** pulses enables CK**2**, completion of CK**2** pulses enables CK**3**, and completion of CK**3** pulses enables CK**4**. Finally, completion of CK**4** pulses enables the GSE signal to switch from capture to shift cycle.

The only difference between these two techniques is that the former uses clock edges to trigger the next operation, the latter uses signal levels to enable the next operation. In practice, a mixed approach can be employed. Since a daisy-chain or token-ring approach is used, the multiple-capture DFT system allows testing of any frequency domain at a reduced clock speed when this particular frequency domain cannot operate at-speed. This is very common in testing high-speed integrated circuits, such as microprocessors and networking chips, where different clock speeds of chips are sold at different prices. In addition, due to its ease of control, this approach further allows at-speed scan-test simply using internally reconfigured capture clocks. Thus, a low-cost tester (ATE) can be used for at-speed scan-test, in addition to at-speed self-test.

The multiple-capture DFT system in the present invention further comprises applying an ordered sequence of capture clocks and operating each capture clock at its selected clock speed in the capture operation (cycle). The ordered sequence of capture clocks is applied to the circuit under test one-by-one using the daisy-chain clock-triggering or token-ring clock-enabling technique. The order of these capture clocks is further programmable, when it's required to increase the circuit's fault coverage. Each capture clock can be also disabled or chosen to facilitate fault diagnosis. In addition, when two clock domains do not interact with each other, they can be tested simultaneously to shorten the capture cycle time.

Each capture clock of the present invention further comprises one or more clock pulses. The number of clock pulses is further programmable. When self-test is employed, the multiple-capture DFT system is usually placed inside the integrated circuit and, thus, all capture clocks are generated internally. When scan-test is employed, the multiple-capture DFT system is usually resided in an ATE and, thus, all capture clocks are controlled externally. However, for at-speed scan-test, it's often required to capture output responses using its respective operating frequency within each clock domain. The present invention further comprises any method or apparatus for allowing use of internally-generated or externally-controlled capture clocks for at-speed scan-test or self-test.

After the capture operation is completed, all output responses captured at all scan cells are compacted internally to signatures or shifted out to the multiple-capture DFT system for direct comparison. The compact or compare operation occurs concurrently with the shift operation, and the process of shift, capture, and compact/compare operations shall continue until a predetermined limiting criteria, such as completion of all self-test or scan-test cycles, is reached. Finally, the multiple-capture DFT system will compare the signatures against expected signatures when the compact operation is employed during self-test or scan-test. Such comparison can be done either in the integrated circuit with a built-in comparator or in an ATE by shifting the final signatures out for analysis.

In the present invention, both self-test and scan-test techniques are employed to detect or locate stuck-at and delay faults. The stuck-at faults further comprise other stuck-type faults, such as open and bridging faults. The delay faults further comprise other non-stuck-type delay faults, such as transition (gate-delay), multiple-cycle delay, and path-delay faults. In addition, each scan cell can be a multiplexed D flip-flop or a level sensitive latch, and the integrated circuit or circuit assembly under test can be a full-scan or partial-scan design.

In general, it is only required to apply one clock pulse and two consecutive clock pulses to test stuck-at faults and delay faults within one clock domain, respectively. Multiple-cycle paths present within one clock domain and between clock domains, however, require waiting for a number of clock cycles for capturing. To test multiple-cycle paths within clock domains, the present invention further comprise applying only one clock pulse to test these multiple-cycle paths within each clock domain by reducing the frequency of that domain's capture clock speed to the level where only paths of equal cycle latency (cycle delays) are captured at its intended rated clock speed one at a time. To test multiple-cycle paths between two clock domains, the present invention further comprise adjusting the relative clock delay along the paths to the level where the crossing-boundary multiple-cycle paths are captured at its intended rated clock speed.

To summarize, the present invention centers on using one global scan enable (GSE) signal for driving all scan enable (SE) signals at a reduced clock speed and applying an ordered sequence of capture clocks for capturing output responses in both self-test and scan-test modes. The present invention assumes that the integrated circuit or circuit assembly must contain two or more clock domains each controlled by one capture clock. During self-test, each capture clock shall contain one or more clock pulses, and during scan-test, one of the capture clocks must contain two or more clock pulses.

Due to its ease of control on the scan enable and capture clock signals, the multiple-capture DFT system of the present invention can now be easily realized by an apparatus and synthesized using computer-aided design (CAD) tools. The present invention further comprises such a CAD system for synthesizing the apparatus and verifying its correctness using combinational fault simulation and combinational ATPG in self-test or scan-test mode.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, advantages and features of the invention will become more apparent when considered with the following specification and accompanying drawings wherein:

FIG. **1** shows an example full-scan or partial-scan design with 4 clock domains and 4 system clocks, where a multiple-capture DFT system in accordance with the present invention is used to detect or locate stuck-at faults at a reduced clock speed in self-test or scan-test mode.

FIG. **2** shows a multiple-capture DFT system with multiple PRPG-MISR pairs, in accordance with the present invention, which is used at a reduced clock speed in self-test mode to detect or locate stuck-at faults in the design given in FIG. **1**.

FIG. **3** shows a timing diagram of the full-scan design given in FIG. **1**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and stuck-

at faults crossing clock domains in self-test mode. The chain of control events is also shown.

FIG. **4** shows a timing diagram of the full-scan design given in FIG. **1**, in accordance with the present invention, where a shortened yet ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and stuck-at faults crossing clock domains in self-test mode.

FIG. **5** shows a timing diagram of the full-scan design given in FIG. **1**, in accordance with the present invention, where an expanded yet ordered sequence of capture clocks is used to detect or locate other stuck-type faults within each clock domain and other stuck-type faults crossing clock domains in self-test or scan-test mode.

FIG. **6** shows a timing diagram of the partial-scan design given in FIG. **1**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **7** shows an example full-scan or partial-scan design with 4 clock domains and 4 system clocks, where a multiple-capture DFT system in accordance with the present invention is used to detect or locate stuck-at, delay, and multiple-cycle delay faults at its desired clock speed in self-test or scan-test mode.

FIG. **8** shows a multiple-capture DFT system with multiple PRPG-MISR pairs, in accordance with the present invention, which is used at its desired clock speed in self-test or scan-test mode to detect or locate stuck-at, delay, and multiple-cycle delay faults in the design given in FIG. **7**.

FIG. **9** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and stuck-at faults crossing clock domains in self-test mode.

FIG. **10** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode. The chain of control events is also shown.

FIG. **11** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where a shortened yet ordered sequence of capture clocks is used to detect or locate delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **12** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and delay faults crossing clock domains in self-test or scan-test mode.

FIG. **13** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate delay faults within each clock domain and delay faults crossing clock domains in self-test or scan-test mode.

FIG. **14** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where a reordered sequence of capture clocks is used to detect or locate delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **15** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an expanded yet ordered sequence of capture clocks is used to detect or locate additional delay faults within each clock domain and additional stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **16** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate 2-cycle delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **17** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate 2-cycle delay faults within each clock domain and 2-cycle delay faults crossing clock domains in self-test or scan-test mode.

FIG. **18** shows a timing diagram of the partial-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate stuck-at faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **19** shows a timing diagram of the partial-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **20** shows a timing diagram of the partial-scan design given in FIG. **7**, in accordance with the present invention, where an ordered sequence of capture clocks is used to detect or locate 2-cycle delay faults within each clock domain and stuck-at faults crossing clock domains in self-test or scan-test mode.

FIG. **21** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where the capture clock CK**2** during the capture cycle is chosen to diagnose faults captured by CK**2** in self-test or scan-test mode.

FIG. **22** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where the capture clocks CK**1** and CK**3** during the capture cycle are chosen to diagnose faults captured by CK**1** and CK**3** in self-test or scan-test mode.

FIG. **23** shows a timing diagram of the full-scan design given in FIG. **1**, in accordance with the present invention, where all capture clocks during the shift cycle are skewed to reduce power consumption.

FIG. **24** shows a multiple-capture CAD system in accordance with the present invention, where a CAD system is used to implement the multiple-capture DFT technique on a full-scan or partial-scan design in self-test mode.

FIG. **25** shows a multiple-capture CAD system in accordance with the present invention, where a CAD system is used to implement the multiple-capture DFT technique on a full-scan or partial-scan design in scan-test mode.

DETAILED DESCRIPTION OF THE DRAWINGS

The following description is of presently contemplated as the best mode of carrying out the present invention. This description is not to be taken in a limiting sense but is made merely for the purpose of describing the principles of the invention. The scope of the invention should be determined by referring to the appended claims.

FIG. **1** shows an example full-scan or partial-scan design with a multiple-capture DFT system, of one embodiment of the invention. The design **133** contains 4 clock domains, CD**1** **102** to CD**4** **105**, and **4** system clocks, CK**1** **111** to CK**4** **120**. Each system clock controls one clock domain. CD**1** **102** and CD**2** **103** talk to each other via a crossing clock-domain logic

block CCD**1** **106**; CD**2** **103** and CD**3** **104** talk to each other via a crossing clock-domain logic block CCD**2** **107**; and CD**3** **104** and CD**4** **105** talk to each other via a crossing clock-domain logic block CCD**3** **108**.

The 4 clock domains, CD**1** **102** to CD**4** **105**, are originally designed to run at 150 MHz, 100 MHz, 100 MHz, and 66 MHz, respectively. However, in this example, since a DFT (self-test or scan-test) technique is only employed to detect or locate stuck-at faults in the design **133**, all system clocks, CK**1** **111** to CK**4** **120**, are reconfigured to operate at 10 MHz. The reconfigured system clocks are called capture clocks.

During self-test or scan-test, the multiple-capture DFT system **101** will take over the control of all stimuli, **109**, **112**, **115**, and **118**, all system clocks, CK**1** **111** to CK**4** **120**, and all output responses, **110**, **113**, **116**, and **119**.

During the shift operation, the multiple-capture DFT system **101** first generates and shifts pseudorandom or predetermined stimuli through **109**, **112**, **115**, and **118** to all scan cells SC in all scan chains SCN within the 4 clock domains, CD**1** **102** to CD**4** **105**, simultaneously. The multiple-capture DFT system **101** shall wait until all stimuli, **109**, **112**, **115**, and **118**, have been shifted into all scan cells SC. It should be noted that, during the shift operation, the capture clock can be operated either at its rated clock speed (at-speed) or at a desired clock speed.

After the shift operation is completed, an ordered sequence of capture clocks is applied to all clock domains, CD**1** **102** to CD**4** **105**. During the capture operation, each capture clock can operate at its rated clock speed (at-speed) or at a reduced speed (slow-speed), and can be generated internally or controlled externally. In this example, all system clocks, CK**1** **111** to CK**4** **120**, are reconfigured to operate at a reduced frequency of 10 MHz.

After the capture operation is completed, the output responses captured at all scan cells SC are shifted out through responses **110**, **113**, **116**, and **119** to the multiple-capture DFT system **101** for compaction during the compact operation or direct comparison during the compare operation.

Based on FIG. **1**, the timing diagrams given in FIGS. **3** to **6** are used to illustrate that, by properly ordering the sequence of capture clocks and by adjusting relative inter-clock delays, stuck-at faults within each clock domain and crossing clock domains can be detected or located in self-test or scan-test mode. Please note that different ways of ordering the sequence of capture clocks and adjusting relative inter-clock delays will result in different faults to be detected or located.

FIG. **2** shows a multiple-capture DFT system with three PRPG-MISR pairs, of one embodiment of the invention, used to detect or locate stuck-at faults in the design **133** given in FIG. **1** in self-test mode.

Pseudorandom pattern generators (PRPGs), **211** to **213**, are used to generate pseudorandom patterns. Phase shifters, **214** to **216**, are used to break the dependency between different outputs of the PRPGs. The bit streams coming from the phase shifters become test stimuli, **109**, **112**, **115**, and **118**.

Space compactors, **217** to **219**, are used to reduce the number of bit streams in test responses, **110**, **113**, **116**, and **119**. Space compactors are optional and are only used when the overhead of a MISR becomes a concern. The outputs of the space compactors are then compressed by multiple input signature registers (MISRs), **220** to **222**. The contents of MISRs after all test stimuli are applied become signatures, **236** to **238**. The signatures are then be compared by comparators, **223** to **225**, with corresponding expected values. The error indicator **226** is used to combine the individual pass/fail signals, **242** to **244**, a global pass/fail signal **245**. Alternatively, the signatures in MISRs **220** to **222** can be shifted to the outside of the design for comparison through a single scan chain composed of elements **223**, **239**, **224**, **240**, **225**, and **241**.

The central self-test controller **202** controls the whole test process by manipulating individual scan enable signals, **204** to **207**, and by reconfiguring capture clocks, CK**1** **111** to CK**4** **120**. Especially, the scan enable signals, **204** to **207**, can be controlled by one global scan enable signal GSE **201**, which can be a slow signal in that it does not have to settle down in half of the cycle of any clock applied to any clock domain. Some additional control signals **203** are needed to conduct other control tasks.

The clock domains **103** and **104**, which are operated at the same frequency, share the same pair of PRPG **212** and MISR **221**. It should be noted that the skew between the clocks CK**2** **114** and CK**3** **117** should be properly managed to prevent any timing violations during the shift operation and any races during the capture operation.

All storage elements in PRPGs, **211** to **213**, and MISRs, **220** to **222**, can be connected into a scan chain from which predetermined patterns can be shifted in for reseeding and computed signatures can be shifted out for analysis. This configuration helps in increasing fault coverage and in facilitating fault diagnosis.

FIG. **3** shows a timing diagram of a full-scan design given in FIG. **1**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test mode. The timing diagram **300** shows the sequence of waveforms of the 4 capture clocks, CK**1** **111** to CK**4** **120**, operating at the same frequency.

During each shift cycle **310**, a series of pulses of 10 MHz are applied through capture clocks, CK**1** **111** to CK**4** **120**, to shift stimuli to all scan cells within all clock domains, CD**1** **102** to CD**4** **105**.

During each capture cycle **311**, 4 sets of capture clock pulses are applied in the following order: First, one capture pulse is applied to CK**1** **111** to detect or locate stuck-at faults within the clock domain CD**1** **102**. Second, one capture pulse is applied to CK**2** **114** to detect or locate stuck-at faults within the clock domain CD**2** **103**. Third, one capture pulse is applied to CK**3** **117** to detect or locate stuck-at faults within the clock domain CD**3** **104**. Fourth, one capture pulse is applied to CK**4** **120** to detect or locate stuck-at faults within the clock domain CD**4** **105**.

In addition, the stuck-at faults which can be reached from lines **121**, **125**, and **129** in the crossing clock-domain logic blocks CCD**1** **106** to CCD**3** **108**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **307** between the rising edge of the capture pulse of CK**1** **111** and the rising edge of the capture pulse of CK**2** **114** must be adjusted so that no races or timing violations would occur while the output responses **123** are captured through the crossing clock-domain logic block CCD**1** **106**.

The same principle applies to the relative clock delay **308** between CK**2** **114** and CK**3** **117**, and the relative clock delay **309** between CK**3** **117** and CK**4** **120** for capturing output responses, **127** and **131**, through CCD**2** **107** and CCD**3** **108**, respectively.

It should be noticed that, generally, during each shift cycle, any capture clock is allowed to operate at its desired or a reduced clock speed. In addition, it is not necessary that all capture clocks must operate at the same clock speed. Furthermore, to reduce peak power consumption during the shift cycle, all capture clocks can be skewed so that at any given time only scan cells within one clock domain can change

states. One global scan enable signal GSE **201**, operated at a reduced clock speed, can also be used, when requested, to switch the test operation from the shift cycle to the capture cycle, and vice versa.

The daisy-chain clock-triggering technique is used to generate and order the sequence of capture clocks one after the other in the following way: The rising edge of the last pulse in the shift cycle triggers the event **301** of applying 0 to the global scan enable GSE **201**, switching the test operation from the shift cycle to the capture cycle. The falling edge of GSE **201** triggers the event **302** of applying one capture pulse to CK**1 111**. Similarly, the rising edge of the capture pulse of CK**1 111** triggers the event **303** of applying one capture pulse to CK**2 114**, the rising edge of the capture pulse of CK**2 114** triggers the event **304** of applying one capture pulse to CK**3 117**, and the rising edge of the capture pulse of CK**3 117** triggers the event **305** of applying one capture pulse to CK**4 120**. Finally, the rising edge of the capture pulse of CK**4 120** triggers the event **306** of applying 1 to the global scan enable GSE **201**, switching the test operation from the capture cycle to the shift cycle. This daisy-chain clock-triggering technique is also used to order the sequence of capture clocks in FIGS. **4** to **6**.

FIG. **4** shows a timing diagram of a full-scan design given in FIG. **1**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with a shortened yet ordered sequence of capture clocks in self-test mode. The timing diagram **400** shows the sequence of waveforms of the 4 capture clocks, CK**1 111** to CK**4 120**, operating at the same frequency.

During each shift cycle **402**, a series of clock pulses of 10 MHz are applied through capture clocks, CK**1 111** to CK**4 120**, to shift stimuli to all scan cells within all clock domains, CD**1 102** to CD**4 105**.

During each capture cycle **403**, two sets of capture clock pulses are applied in the following order: First, one capture pulse is applied to CK**1 111** and CK**3 117** simultaneously to detect or locate stuck-at faults within the clock domain CD**1 102** and CD**3 104**, respectively. Second, one capture pulse is applied to CK**2 114** and CK**4 120** simultaneously to detect or locate stuck-at faults within the clock domain CD**2 103** and CD**4 105**, respectively.

In addition, the stuck-at faults which can be reached from lines **121**, **128**, and **129** in the crossing clock-domain logic blocks CCD**1 106** to CCD**3 108**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **401** between the rising edge of the capture pulse for CK**1 111** and CK**3 117** and the rising edge of the capture pulse for CK**2 114** and CK**4 120**, must be adjusted so that no races or timing violations would occur while the output responses, **123**, **126**, and **131**, are captured through the crossing clock-domain logic blocks CCD**1 106** to CCD**3 108**.

FIG. **5** shows a timing diagram of a full-scan design in FIG. **1** of one embodiment of the invention for detecting or locating other stuck-type faults within each clock domain and other stuck-type faults crossing clock domains with an expanded yet ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **500** shows the sequence of waveforms of the 4 capture clocks, CK**1 111** to CK**4 120**, operating at the same frequency.

During each shift cycle **503**, a series of clock pulses of 10 MHz are applied through capture clocks, CK**1 111** to CK**4 120**, to shift stimuli to all scan cells within all clock domains, CD**1 102** to CD**4 105**.

During each capture cycle **504**, two sets of capture clock pulses are applied in the following order: First, two capture pulses are applied to CK**1 111** and CK**3 117**, simultaneously. Second, one capture pulse is applied to CK**2 114** and CK**4 120**, simultaneously. Stuck-at faults in all crossing clock-domain combinations, from **121** to **123**, from **124** to **122**, from **125** to **127**, from **128** to **126**, from **129** to **131**, from **132** to **130**, can be detected or located if the following condition is satisfied: The relative clock delay **501** between the rising edge of the first capture pulse of CK**1 111** and CK**3 117** and the rising edge of the capture pulse of CK**2 114** and CK**4 120** must be adjusted so that no races or timing violations would occur while the output responses **123**, **126**, and **131** are captured through the crossing clock-domain logic block CCD**1 106** to CCD**3 108**, respectively. The relative clock delay **502** between the rising edge of the capture pulse of CK**2 114** and CK**4 120** and the second capture pulse of CK**1 111** and CK**3 117** must be adjusted so that no races or timing violations would occur while the output responses **122**, **127**, and **130** are captured through the crossing clock-domain logic block CCD**1 106** to CCD**3 108**, respectively.

FIG. **6** shows a timing diagram of a feed-forward partial-scan design given in FIG. **1**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with a shortened yet ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that the clock domains CD**1 102** to CD**4 105** contain a number of un-scanned storage cells that form a sequential depth of no more than 2. The timing diagram **600** shows the sequence of waveforms of the 4 capture clocks, CK**1 111** to CK**4 120**, operating at the same frequency.

During each shift cycle **606**, a series of clock pulses of 10 MHz are applied through capture clocks, CK**1 111** to CK**4 120**, to shift stimuli to all scan cells within all clock domains, CD**1 102** to CD**4 105**.

During each capture cycle **607**, two sets of capture clock pulses are applied in the following order: First, three pulses of 10 MHz, two being functional pulses and one being a capture pulse, are applied to CK**1 111** and CK**3 117** simultaneously to detect or locate stuck-at faults within the clock domain CD**1 102** and CD**3 104**, respectively. Second, three pulses of 10 MHz, two being functional pulses and one being a capture pulse, are applied to CK**2 114** and CK**4 120** simultaneously to detect or locate stuck-at faults within the clock domain CD**2 103** and CD**4 105**, respectively.

In addition, the stuck-at faults which can be reached from lines **121**, **128**, and **129** in the crossing clock-domain logic blocks CCD**1 106** to CCD**3 108**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **603** between the rising edge of the capture pulse for CK**1 111** and CK**3 117** and the rising edge of the capture pulse for CK**2 114** and CK**4 120** must be adjusted so that no races or timing violations would occur while the output responses, **123**, **126**, and **131**, are captured through the crossing clock-domain logic blocks CCD**1 106** to CCD**3 108**.

FIG. **7** shows an example full-scan or partial-scan design with a multiple-capture DFT system, of one embodiment of the invention. The design **733** is the same as the design **133** given in FIG. **1**. Same as in FIG. **1**, the 4 clock domains, CD**1 702** to CD**4 705**, are originally designed to run at 150 MHz, 100 MHz, 100 MHz, and 66 MHz, respectively. The only difference from FIG. **1** is that these clock frequencies will be used directly without alternation in order to implement at-

speed self-test or scan-test for stuck-at, delay, and multiple-cycle delay faults within each clock domain and crossing clock domains.

Based on FIG. **7**, the timing diagrams given in FIGS. **9** to **20** are used to illustrate that, by properly ordering the sequence of capture pulses and by adjusting relative inter-clock delays, the at-speed detection or location of stuck-at, delay, and multiple-cycle delay faults within each clock domain and crossing clock domains can be achieved in self-test or scan-test mode. Please note that different ways of ordering the sequence of capture pulses and adjusting relative inter-clock delays will result in different faults to be detected or located.

FIG. **8** shows a multiple-capture DFT system with three PRPG-MISR pairs, of one embodiment of the invention, used in self-test or scan-test mode to detect or locate stuck-at, delay, and multiple-cycle delay faults in the design given in FIG. **7**. The composition and operation of the multiple-capture DFT system is basically the same as the one given in FIG. **2**. There are two major differences: one is that, in this example, the original clock frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are used directly without alternation in order to implement at-speed self-test or scan-test. The other is that more care needs to be taken in the physical design of scan chains, etc., in this example.

The clock domains **703** and **704**, which are operated at the same frequency, share the same pair of PRPG **812** and MISR **821**. It should be noted that the skew between the clocks CK**2** **714** and CK**3** **717** should be properly managed to prevent any timing violations during the shift operation and any races during the capture operation.

All storage elements in PRPGs, **811** to **813**, and MISRs, **820** to **822**, can be connected into a scan chain from which predetermined patterns can be shifted in for reseeding and computed signatures can be shifted out for analysis. This configuration helps in increasing fault coverage and in facilitating fault diagnosis.

FIG. **9** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test mode. The timing diagram **900** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies. This timing diagram is basically the same as the one given in FIG. **3** except the capture clocks, CK**1** **711** to CK**4** **720**, run at 150 MHz, 100 MHz, 100 MHz, and 66 MHz, respectively, in both shift and capture cycles, instead of 10 MHz as in FIG. **3**.

FIG. **10** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating delay faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1000** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1014**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1015**, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of 150 MHz are applied to CK**1** **711** to detect or locate delay faults within the clock domain CD**1** **702**. Second, two capture pulses of 100 MHz are applied to CK**2** **714** to detect or locate delay faults within the clock domain CD**2** **703**. Third, two capture pulses of 100 MHz are applied to CK**3** **717** to detect or locate delay faults within the clock domain CD**3** **704**. Fourth, two capture pulses of 66 MHz are applied to CK**4** **720** to detect or locate delay faults within the clock domain CD**4** **705**.

In addition, the stuck-at faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1008** between the rising edge of the second capture pulse of CK**1** **711** and the rising edge of the first capture pulse of CK**2** **714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCD**1** **706**.

The same principle applies to the relative clock delay **1010** between CK**2** **714** and CK**3** **717**, and the relative clock delay **1012** between CK**3** **717** and CK**4** **720** for capturing the output responses, **727** and **731**, through CCD**2** **707** and CCD**3** **708**, respectively.

The daisy-chain clock-triggering technique is used to generate and order the sequence of capture clocks one after the other in the following way: The rising edge of the last pulse in the shift cycle triggers the event **1001** of applying **0** to the global scan enable GSE **801**, switching the test operation from the shift cycle to the capture cycle. The falling edge of GSE **801** triggers the event **1002** of applying two capture pulses to CK**1** **711**. Similarly, the rising edge of the second capture pulse of CK**1** **711** triggers the event **1003** of applying two capture pulses to CK**2** **714**, the rising edge of the second capture pulse of CK**2** **714** triggers the event **1004** of applying two capture pulses to CK**3** **717**, and the rising edge of the second capture pulse of CK**3** **717** triggers the event **1005** of applying two capture pulses to CK**4** **720**. Finally, the rising edge of the second capture pulse of CK**4** **720** triggers the event **1006** of applying 1 to the global scan enable GSE **801**, switching the test operation from the capture cycle to the shift cycle. This daisy-chain clock-triggering technique is also used to order the sequence of capture clocks in FIG. **9** and FIGS. **11** to **20**.

FIG. **11** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating delay faults within each clock domain and stuck-at faults crossing clock domains with a shortened yet ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1100** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1108**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1109**, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of frequency 150 MHz are applied to CK**1** **711** and two clock pulses of frequency 100 MHz are applied to CK**3** **717**, simultaneously, to detect or locate delay faults within the clock domain CD**1** **702** and CD**3** **704**, respectively. Second, two capture pulses of frequency 100 MHz are applied to CK**2** **714** and two capture pulses of frequency 66 MHz are applied to CK**4** **720**, simultaneously, to detect or locate delay faults within the clock domain CD**2** **703** and CD**4** **705**, respectively.

In addition, the stuck-at faults which can be reached from lines **721**, **728**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition

is satisfied: The relative clock delay **1102** between the rising edge of the second capture pulse of CK**1 711** and the rising edge of the first capture pulse of CK**2 714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCD**1 706**.

The same principle applies to the relative clock delay **1104** between CK**3 717** and CK**2 714**, and the relative clock delay **1106** between CK**3 717** and CK**4 720** for capturing the output responses, **726** and **731**, through CCD**2 707** and CCD**3 708**, respectively.

FIG. **12** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and delay faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1200** shows the sequence of waveforms of the 4 capture clocks, CK**1 711** to CK**4 720**, operating at different frequencies.

During each shift cycle **1204**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1 711** to CK**4 720**, to shift stimuli to all scan cells within all clock domains, CD**1 702** to CD**4 705**.

During each capture cycle **1205**, 4 sets of capture clock pulses are applied in the following order: First, one capture pulse of 150 MHz is applied to CK**1 711** to detect or locate stuck-at faults within the clock domain CD**1 702**. Second, one capture pulse of 100 MHz is applied to CK**2 714** to detect or locate stuck-at faults within the clock domain CD**2 703**. Third, one capture pulse of 100 MHz is applied to CK**3 717** to detect or locate stuck-at faults within the clock domain CD**3 704**. Fourth, one capture pulse of 66 MHz is applied to CK**4 720** to detect or locate stuck-at faults within the clock domain CD**4 705**.

In addition, the delay faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD**1 706** to CCD**3 708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delays **1201** between the rising edge of the capture pulse of CK**1 711** and the rising edge of the capture pulse of CK**2 714** must be adjusted to meet the at-speed timing requirements for paths from **721** to **723**. Similarly, the relative clock delay **1202** between CK**2 714** and CK**3 717**, and the relative clock delay **1203** between CK**3 717** and CK**4 720**, must be adjusted to meet the at-speed timing requirements for paths from **725** to **727**, and paths from **729** to **731**, respectively.

FIG. **13** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating delay faults within each clock domain and delay faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1300** shows the sequence of waveforms of the 4 capture clocks, CK**1 711** to CK**4 720**, operating at different frequencies.

During each shift cycle **1308**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1 711** to CK**4 720**, to shift stimuli to all scan cells within all clock domains, CD**1 702** to CD**4 705**.

During each capture cycle **1309**, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of 150 MHz are applied to CK**1 711** to detect or locate delay faults within the clock domain CD**1 702**. Second, two capture pulses of 100 MHz are applied to CK**2 714** to detect or locate delay faults within the clock domain CD**2 703**. Third, two capture pulses of 100 MHz are applied to CK**3 717** to detect or locate delay faults within the clock domain CD**3 704**. Fourth, two capture pulses of 66 MHz are applied to CK**4 720** to detect or locate delay faults within the clock domain CD**4 705**.

In addition, the delay faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD**1 706** to CCD**3 708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1302** between the rising edge of the second capture pulse of CK**1 711** and the rising edge of the first capture pulse of CK**2 714** must be adjusted to meet the at-speed timing requirements for paths from **721** to **723**. Similarly, the relative clock delay **1304** between CK**2 714** and CK**3 717**, and the relative clock delay **1306** between CK**3 717** and CK**4 720**, must be adjusted to meet the at-speed timing requirements for paths from **725** to **727**, and paths from **729** and **731**, respectively.

FIG. **14** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating delay faults within each clock domain and stuck-at faults crossing clock domains with a reordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1400** shows the sequence of waveforms of the 4 capture clocks, CK**1 711** to CK**4 720**, operating at different frequencies.

During each shift cycle **1408**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1 711** to CK**4 720**, to shift stimuli to all scan cells within all clock domains, CD**1 702** to CD**4 705**.

During each capture cycle **1409**, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of 66 MHz are applied to CK**4 720** to detect or locate delay faults within the clock domain CD**4 705**. Second, two capture pulses of 100 MHz are applied to CK**3 717** to detect or locate delay faults within the clock domain CD**3 704**. Third, two capture pulses of 100 MHz are applied to CK**2 714** to detect or locate delay faults within the clock domain CD**2 703**. Fourth, two capture pulses of 150 MHz are applied to CK**1 711** to detect or locate delay faults within the clock domain CD**1 702**.

In addition, the stuck-at faults which can be reached from lines **724**, **728**, and **732** in the crossing clock-domain logic blocks CCD**1 706** to CCD**3 708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1402** between the rising edge of the second capture pulse of CK**4 720** and the rising edge of the first capture pulse of CK**3 717** must be adjusted so that no races or timing violations would occur while the output responses **730** are captured through the crossing clock-domain logic block CCD**3 708**.

The same principle applies to the relative clock delay **1404** between CK**3 717** and CK**2 714**, and the relative clock delay **1406** between CK**2 714** and CK**1 711** for capturing output responses, **726** and **722**, through CCD**2 707** and CCD**1 706**, respectively

FIG. **15** shows a timing diagram of a full-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating additional delay faults within each clock domain and additional stuck-at faults crossing clock domains with an expanded yet ordered sequence of capture clocks in self-test or scan-test mode. The timing diagram **1500** shows the sequence of waveforms of the 4 capture clocks, CK**1 711** to CK**4 720**, operating at different frequencies.

During each shift cycle **1514**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66

MHz, are applied through capture clocks, CK1 711 to CK4 720, to shift stimuli to all scan cells within all clock domains, CD1 702 to CD4 705.

During each capture cycle 1515, seven sets of double-capture pulses are applied in the following order: First, two capture pulses of 150 MHz are applied to CK1 711. Second, two capture pulses of 100 MHz are applied to CK2 714. Third, two capture pulses of 100 MHz are applied to CK3 717. Fourth, two capture pulses of 66 MHz are applied to CK4 720. Fifth, two capture pulses of 100 MHz are applied to CK3 717. Sixth, two capture pulses of 100 MHz are applied to CK2 714. Seventh, two capture pulses of 150 MHz are applied to CK1 711.

For the capture clock CK1 711, the second pulse and the third pulse are used to launch the transition needed for detecting or locating delay faults within the clock domain CD1 702. Since the transition is generated by two close-to-functional patterns, the risk of activating a false path is lower. In addition, additional delay faults within the clock domain CD1 702 can be detected or located by the transition. The same results also apply to the clock domains CD2 703 and CD3 704.

In addition, the stuck-at faults which can be reached from lines 724, 728, and 732 in the crossing clock-domain logic blocks CCD1 706 to CCD3 708, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay 1508 between the rising edge of the second capture pulse of CK4 720 and the rising edge of the first capture pulse of CK3 717 must be adjusted so that no races or timing violations would occur while the output responses 730 are captured through the crossing clock-domain logic block CCD3 708.

The same principle applies to the relative clock delay 1510 between CK3 717 and CK2 714, and the relative clock delay 1512 between CK2 714 and CK1 711 for capturing output responses, 726 and 722, through CCD2 707 and CCD1 706, respectively.

FIG. 16 shows a timing diagram of a full-scan design given in FIG. 7, of one embodiment of the invention for detecting or locating 2-cycle delay faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that some paths in the clock domains, CD1 702 to CD4 705, need two cycles for signals to pass through. The timing diagram 1600 shows the sequence of waveforms of the 4 capture clocks, CK1 711 to CK4 720, operating at different frequencies.

During each shift cycle 1608, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK1 711 to CK4 720, to shift stimuli to all scan cells within all clock domains, CD1 702 to CD4 705.

During each capture cycle 1609, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of 75 MHz (half of 150 MHz) are applied to CK1 711 to detect or locate 2-cycle delay faults within the clock domain CD1 702. Second, two capture pulses of 50 MHz (half of 100 MHz) are applied to CK2 714 to detect or locate 2-cycle delay faults within the clock domain CD2 703. Third, two capture pulses of 50 MHz (half of 100 MHz) are applied to CK3 717 to detect or locate 2-cycle delay faults within the clock domain CD3 704. Fourth, two capture pulses of 33 MHz (half of 66 MHz) are applied to CK4 720 to detect or locate 2-cycle delay faults within the clock domain CD4 705.

In addition, the stuck-at faults which can be reached from lines 721, 725, and 729 in the crossing clock-domain logic blocks CCD1 706 to CCD3 708, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay 1602 between the rising edge of the second capture pulse of CK1 711 and the rising edge of the first capture pulse of CK2 714 must be adjusted so that no races or timing violations would occur while the output responses 723 are captured through the crossing clock-domain logic block CCD1 706.

The same principle applies to the relative clock delay 1604 between CK2 714 and CK3 717, and the relative clock delay 1606 between CK3 717 and CK4 720 for capturing output responses, 727 and 731, through CCD2 707 and CCD3 708, respectively.

FIG. 17 shows a timing diagram of a full-scan design given in FIG. 7, of one embodiment of the invention for detecting or locating 2-cycle delay faults within each clock domain and 2-cycle delay faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that some paths in the clock domains, CD1 702 to CD4 705, and the crossing clock-domain logic blocks, CCD1 706 to CCD3 708, need two cycles for signals to pass through. The timing diagram 1700 shows the sequence of waveforms of the 4 capture clocks, CK1 711 to CK4 720, operating at different frequencies.

During each shift cycle 1708, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK1 711 to CK4 720, to shift stimuli to all scan cells within all clock domains, CD1 702 to CD4 705.

During each capture cycle 1709, 4 sets of capture clock pulses are applied in the following order: First, two capture pulses of 75 MHz (half of 150 MHz) are applied to CK1 711 to detect or locate 2-cycle delay faults within the clock domain CD1 702. Second, two capture pulses of 50 MHz (half of 100 MHz) are applied to CK2 714 to detect or locate 2-cycle delay faults within the clock domain CD2 703. Third, two capture pulses of 50 MHz (half of 100 MHz) are applied to CK3 717 to detect or locate 2-cycle delay faults within the clock domain CD3 704. Fourth, two capture pulses of 33 MHz (half of 66 MHz) are applied to CK4 720 to detect or locate 2-cycle delay faults within the clock domain CD4 705.

In addition, the 2-cycle delay faults which can be reached from lines 721, 725, and 729 in the crossing clock-domain logic blocks CCD1 706 to CCD3 708, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay 1702 between the rising edge of the second capture pulse of CK1 711 and the rising edge of the first capture pulse of CK2 714 must be adjusted to meet the 2-cycle timing requirements for paths from 721 to 723. Similarly, the relative clock delay 1704 between CK2 714 and CK3 717, and the relative clock delay 1706 between CK3 717 and CK4 720, must be adjusted to meet the 2-cycle timing requirements for paths from 725 to 727, and paths from 729 and 731, respectively.

FIG. 18 shows a timing diagram of a feed-forward partial-scan design given in FIG. 7, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that the clock domains CD1 702 to CD4 705 contain a number of un-scanned storage cells that form a sequential depth of no more than 2. The timing diagram 1800 shows the sequence of waveforms of the 4 capture clocks, CK1 711 to CK4 720, operating at different frequencies.

During each shift cycle 1812, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK1 711 to CK4 720, to shift stimuli to all scan cells within all clock domains, CD1 702 to CD4 705.

During each capture cycle **1813**, 4 sets of capture clock pulses are applied in the following order: First, three pulses of 150 MHz, two being functional pulses and one being a capture pulse, are applied to CK**1** **711** to detect or locate stuck-at faults within the clock domain CD**1** **702**. Second, three pulses of 100 MHz, two being functional pulses and one being a capture pulse, are applied to CK**2** **714** to detect or locate stuck-at faults within the clock domain CD**2** **703**. Third, three pulses of 100 MHz, two being functional pulses and one being a capture pulse, are applied to CK**3** **717** to detect or locate stuck-at faults within the clock domain CD**3** **704**. Fourth, three pulses of frequency 66 MHz, two being functional pulses and one being a capture pulse, are applied to CK**4** **717** to detect or locate stuck-at faults within the clock domain CD**4** **705**.

In addition, the stuck-at faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1803** between the rising edge of the second capture pulse of CK**1** **711** and the rising edge of the first capture pulse of CK**2** **714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCD**1** **706**.

The same principle applies to the relative clock delay **1806** between CK**2** **714** and CK**3** **717**, and the relative clock delay **1809** between CK**3** **717** and CK**4** **720** for capturing output responses, **727** and **731**, through CCD**2** **707** and CCD**3** **708**, respectively.

FIG. **19** shows a timing diagram of a feed-forward partial-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating delay faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that the clock domains CD**1** **702** to CD**4** **705** contain a number of un-scanned storage cells that form a sequential depth of no more than 2. The timing diagram **1900** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **1916**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **1917**, 4 sets of capture clock pulses are applied in the following order: First, 4 pulses of 150 MHz, two being functional pulses and two being capture pulses, are applied to CK**1** **711** to detect or locate delay faults within the clock domain CD**1** **702**. Second, 4 pulses of 100 MHz, two being functional pulses and two being capture pulses, are applied to CK**2** **714** to detect or locate delay faults within the clock domain CD**2** **703**. Third, 4 pulses of 100 MHz, two being functional pulses and two being capture pulses, are applied to CK**3** **717** to detect or locate delay faults within the clock domain CD**3** **704**. Fourth, 4 pulses of 66 MHz, two being functional pulses and two being capture pulses, are applied to CK**4** **720** to detect or locate delay faults within the clock domain CD**4** **705**.

In addition, the stuck-at faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **1904** between the rising edge of the second capture pulse of CK**1** **711** and the rising edge of the first capture pulse of CK**2** **714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCD**1** **706**.

The same principle applies to the relative clock delay **1908** between CK**2** **714** and CK**3** **717**, and the relative clock delay **1912** between CK**3** **717** and CK**4** **720** for capturing output responses, **727** and **731**, through CCD**2** **707** and CCD**3** **708**, respectively.

FIG. **20** shows a timing diagram of a feed-forward partial-scan design given in FIG. **7**, of one embodiment of the invention for detecting or locating 2-cycle delay faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that the clock domains CD**1** **702** to CD**4** **705** contain a number of un-scanned storage cells that form a sequential depth of no more than 2. Also, it is assumed that some paths in the clock domains, CD**1** **702** to CD**4** **705**, need two cycles for signals to pass through. The timing diagram **2000** shows the sequence of waveforms of the 4 capture clocks, CK**1** **711** to CK**4** **720**, operating at different frequencies.

During each shift cycle **2016**, a series of clock pulses of different frequencies, 150 MHz, 100 MHz, 100 MHz, and 66 MHz, are applied through capture clocks, CK**1** **711** to CK**4** **720**, to shift stimuli to all scan cells within all clock domains, CD**1** **702** to CD**4** **705**.

During each capture cycle **2017**, 4 sets of capture clock pulses are applied in the following order: First, 4 pulses, two being functional pulses of 150 MHz and two being capture pulses of 75 MHz (half of 150 MHz), are applied to CK**1** **711** to detect or locate 2-cycle delay faults within the clock domain CD**1** **702**. Second, **4** pulses, two being functional pulses of 100 MHz and two being capture pulses of 50 MHz (half of 100 MHz), are applied to CK**2** **714** to detect or locate 2-cycle delay faults within the clock domain CD**2** **703**. Third, 4 pulses, two being functional pulses of 100 MHz and two being capture pulses of 50 MHz (half of 100 MHz), are applied to CK**3** **717** to detect or locate 2-cycle delay faults within the clock domain CD**3** **704**. Fourth, 4 pulses, 2 being functional pulses of 66 MHz and 2 being capture pulses of 33 MHz (half of 66 MHz), are applied to CK**4** **720** to detect or locate 2-cycle delay faults within the clock domain CD**4** **705**.

In addition, the stuck-at faults which can be reached from lines **721**, **725**, and **729** in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708**, respectively, are also detected or located simultaneously if the following condition is satisfied: The relative clock delay **2004** between the rising edge of the second capture pulse of CK**1** **711** and the rising edge of the first capture pulse of CK**2** **714** must be adjusted so that no races or timing violations would occur while the output responses **723** are captured through the crossing clock-domain logic block CCD**1** **706**.

The same principle applies to the relative clock delay **2008** between CK**2** **714** and CK**3** **717**, and the relative clock delay **2012** between CK**3** **717** and CK**4** **720** for capturing output responses, **727** and **731**, through CCD**2** **707** and CCD**3** **708**, respectively.

FIG. **21** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where the capture clock CK**2** during the capture cycle is chosen to diagnose faults captured by CK**2** in self-test or scan-test mode.

Fault diagnosis is the procedure by which a fault is located. In order to achieve this goal, it is often necessary to use an approach where a test pattern detects only portion of faults while guaranteeing no other faults are detected. If the test pattern does produce a response that matches the observed response, it can then be declared that the portion must contain

at least one actual fault. Then the same approach to the portion of the faults to further localize the actual faults.

The timing diagram **2100** shows a way to facilitate this approach. In the capture cycle **2107**, two capture pulses of 100 MHz are only applied to the capture clock CK**2** **714** while the other three capture clocks are held inactive. As a result, for delay faults, only those in the clock domain CD**2** **703** are detected. In addition, for stuck-at faults, only those in the crossing clock-domain logic blocks CCD**1** **706** and CCD**2** **707** and the clock domain CD**2** **703** are detected. Obviously, this clock timing helps in fault diagnosis.

FIG. **22** shows a timing diagram of the full-scan design given in FIG. **7**, in accordance with the present invention, where the capture clocks CK**1** and CK**3** during the capture cycle are chosen to diagnose faults captured by CK**1** and CK**3** in self-test or scan-test mode.

The diagram **2200** shows one more timing scheme that can help fault diagnosis as described in the description of FIG. **21**. In the capture cycle **2208**, two capture pulses of 150 MHz are applied to the capture clock CK**1** **711** and two capture pulses of 100 MHz are applied to the capture clock CK**3** **717** while the other two capture clocks are held inactive. As a result, for delay faults, only those in the clock domain CD**1** **702** and CD**3** **704** are detected. In addition, for stuck-at faults, only those in the crossing clock-domain logic blocks CCD**1** **706** to CCD**3** **708** and the clock domains CD**1** **702** and CD**3** **703** are detected. Obviously, this clock timing helps in fault diagnosis.

FIG. **23** shows a timing diagram of the full-scan design given in FIG. **1**, in accordance with the present invention, where all capture clocks during the shift cycle are skewed to reduce power consumption. The timing diagram **2300** only shows the waveforms for the capture clocks CK**1** **111** to CK**4** **120** during the shift cycle. For the capture cycle, any capture timing control methods claimed in this patent can be applied.

During the shift cycle **2305**, clock pulses for the clocks CK**1** **111** to CK**4** **120** are skewed by properly setting the delay **2301** between the shift pulses for the clocks CK**1** **111** and CK**2** **114**, the delay **2302** between the shift pulses for the clocks CK**2** **114** and CK**3** **117**, the delay **2303** between the shift pulses for the clocks CK**3** **117** and CK**4** **120**, the delay **2304** between the shift pulses for the clocks CK**4** **120** and CK**1** **111**. As a result, both peak power consumption and average power consumption are reduced. In addition, during the capture cycle, the PRPG **212** is driven by clock CK**2** **114**, the first-arrived capture clock, and the MISR **221** is driven by clock CK**3** **117**, the last-arrived capture clock, in the shared PRPG-MISR pair **228** in FIG. **2**. Thus, the ordered capture sequence guarantees the correct capture operation when a shared PRPG-MISR pair is used for a plurality of clock domains in self-test mode.

FIG. **24** shows a flow chart of one embodiment of the invention. The multiple-capture self-test computer-aided design (CAD) system **2400** accepts the user-supplied HDL code or netlist **2402** together with the self-test control files **2401** and the chosen foundry library **2403**. The self-test control files **2401** contain all set-up information and scripts required for compilation **2404**, self-test rule check **2406**, self-test rule repair **2507**, and multiple-capture self-test synthesis **2408**. As a result, an equivalent combinational circuit model **2409** is generated. Then, combinational fault simulation **2410** can be performed. Finally, post-processing **2411** is used to produce the final self-test HDL code or netlist **2412** as well as the HDL test benches and ATE test programs **2413**. All reports and errors are saved in the report files **2414**.

The multiple-capture self-test synthesis **2408** uses a hierarchical approach in which it synthesizes a plurality of PRPG-MISR pairs one at a time for each individual clock domain or combined clock domains, then synthesizes a central self-test controller which includes an error indicator, and finally stitches the central self-test controller together with synthesized PRPG-MISR pairs. Each PRPG-MISR pair is composed of a PRPG, an optional phase shifter, an optional space compactor, a MISR, and a comparator. In addition, during PRPG-MISR synthesis, a number of spare scan cells can be inserted into selected clock domains. As a result, the central self-test controller can remain intact even when the need for circuit modification rises at a later stage.

FIG. **25** shows a flow chart of one embodiment of the invention. The multiple-capture scan-test computer-aided design (CAD) system **2500** accepts the user-supplied HDL code or netlist **2502** together with the scan control files **2501** and the chosen foundry library **2503**. The scan control files **2501** contain all set-up information and scripts required for compilation **2504**, scan rule check **2506**, scan rule repair **2507**, and multiple-capture scan synthesis **2508**. As a result, an equivalent combinational circuit model **2509** is generated. Then, combinational ATPG **2510** can be performed. Finally, post-processing **2511** is used to produce the final scan HDL netlist **2512** as well as the HDL test benches and ATE test programs **2513**. All reports and errors are saved in the report files **2514**.

Having thus described presently preferred embodiments of the present invention, it can now be appreciated that the objectives of the invention have been fully achieved. And it will be understood by those skilled in the art that many changes in construction & circuitry, and widely differing embodiments & applications of the invention will suggest themselves without departing from the spirit and scope of the present invention. The disclosures and the description herein are intended to be illustrative and are not in any sense limitation of the invention, more preferably defined in the scope of the invention by the Claims appended hereto and their equivalents.

What is claimed is:

1. An apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in scan-test or self-test mode, where N>1, each clock domain having one capture clock and a plurality of scan cells, each capture clock comprising a plurality of capture clock pulses; said apparatus comprising:

(a) means for generating and shifting-in N test stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during a shift-in operation;

(b) means for applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least a plurality of capture clock pulses from two or more selected capture clocks placed in a sequential order such that all clock domains are never triggered simultaneously during a capture operation; and

(c) means for analyzing output responses of all said scan cells to locate any faults therein.

2. The apparatus of claim **1** wherein all said capture clocks are supplied to said clock domains in a way to reduce power consumption during said self-test or scan-test mode.

3. The apparatus of claim **1**, wherein said capture clock is programmable to contain said selected number of capture clock pulses, in accordance with said ordered sequence of capture clock pulses, for performing said capture operation on all said scan cells within a selected clock domain controlled by said capture clock; wherein all said capture clock

pulses in said capture clock are selectively generated internally or controlled externally, and can be selectively operated at their rated clock speed (at-speed) or at a selected clock speed.

4. The apparatus of claim **3** further comprising means for providing N scan enable (SE) signals each controlling a selected clock domain; wherein all said scan enable (SE) signals are used to switch operations from shift-in to capture, and vice versa; and wherein each said scan enable (SE) signal is selectively generated internally or controlled externally, and can be selectively operated at its rated clock speed or at a selected clock speed.

5. The apparatus of claim **3**, wherein said means for providing N scan enable (SE) signals further comprises means for using one global scan enable (GSE) signal to drive all said scan enable (SE) signals so that said global scan enable (GSE) signal and all said scan enable (SE) signals can be operated at a selected reduced clock speed.

6. The apparatus of claim **1**, wherein there are provided shift clock pulses and said means for generating and shifting-in N test stimuli further comprises means for operating all said shift clock pulses at selected clock speeds or at the same clock speed; wherein all said shift clock pulses are selectively skewed so that at any given time only one or more said scan cells are changing states to reduce power consumption.

7. The apparatus of claim **1**, wherein said means for applying an ordered sequence of capture clock pulses further comprises means for applying said capture clock pulses concurrently to two or more selected clock domains which do not interact with each other or do not have any logic block crossing each other, for detecting or locating said faults in said selected clock domains.

8. The apparatus of claim **1**, wherein said means for applying an ordered sequence of capture clock pulses further comprises means for applying a reversed ordered sequence of capture clock pulses from said ordered sequence of capture clock pulses, for detecting or locating additional faults in said integrated circuit or circuit assembly.

9. The apparatus of claim **1**, wherein said means for applying an ordered sequence of capture clock pulses further comprises means for selectively applying a shortened or expanded ordered sequence of capture clock pulses from said ordered sequence of capture clock pulses, for detecting or locating additional faults in said integrated circuit or circuit assembly.

10. The apparatus of claim **1**, wherein said means for applying an ordered sequence of capture clock pulses further comprises means for disabling all capture clock pulses in one or more capture clocks, to facilitate fault diagnosis.

11. The apparatus of claim **1**, wherein said means for applying an ordered sequence of capture clock pulses further comprises means for selectively operating all said capture clock pulses controlling a selected clock domain at a selected clock speed, for detecting or locating stuck-at faults within said selected clock domain.

12. The apparatus of claim **1**, wherein said means for applying an ordered sequence of capture clock pulses further comprises means for selectively operating all said capture clock pulses controlling a selected clock domain at their rated clock speed, for detecting or locating delay faults within said selected clock domain.

13. The apparatus of claim **1**, wherein said means for applying an ordered sequence of capture clock pulses further comprises means for selectively reducing the speed of all said capture clock pulses controlling a selected clock domain to the level, where delay faults associated with all multiple-cycle paths of equal cycle latency within said selected clock domain are detected or located at a predetermined rated clock speed.

14. The apparatus of claim **1**, wherein said means for applying an ordered sequence of capture clock pulses further comprises means for selectively operating all said capture clock pulses controlling two selected clock domains at selected clock speeds, for detecting or locating stuck-at faults crossing said two selected clock domains.

15. The apparatus of claim **1**, wherein said means for applying an ordered sequence of capture clock pulses further comprises means for selectively adjusting the relative clock delay of two said capture clock pulses controlling two selected clock domains, for detecting or locating delay faults crossing said two selected clock domains.

16. The apparatus of claim **1**, wherein said means for applying an ordered sequence of capture clock pulses further comprises means for selectively adjusting the relative clock delay of two said capture clock pulses controlling two selected clock domains to the level, where delay faults associated with all multiple-cycle paths of equal cycle latency crossing said two selected clock domains are detected or located at a predetermined rated clock speed.

17. The apparatus of claim **1**, wherein said means for applying an ordered sequence of capture clock pulses further comprises means for controlling the relative clock delay between any two adjacent capture clock pulses inside or external to said integrated circuit or circuit assembly.

18. The apparatus of claim **1**, wherein said means for analyzing output responses further comprises means for selectively compacting said N output responses to signatures using a compact operation.

19. The apparatus of claim **1**, wherein means for analyzing output responses further comprises means for comparing said signatures with their expected signatures after a predetermined limiting criterion is reached; wherein said means for comparing said signatures with their expected signatures further comprises means for comparing said signatures inside said integrated circuit or circuit assembly, or shifting-out said signatures for comparison in an ATE (automatic test equipment).

20. The apparatus of claim **1**, wherein said scan cell is selectively a multiplexed D flip-flop or a level-sensitive scan latch, and further wherein said integrated circuit or circuit assembly under test is a full-scan or partial-scan design.

21. The apparatus of claim **1**, wherein said faults further comprise stuck-at faults and delay faults; wherein said stuck-at faults further comprise other stuck-type faults, such as open faults and bridging faults, and wherein said delay faults further comprise other non-stuck-type delay faults, such as transition (gate-delay) faults, multiple-cycle delay faults, and path-delay faults.

* * * * *

CERTIFICATE OF SERVICE

I hereby certify that on August 22, 2014, I caused the foregoing Brief of Appellant SynTest Technologies, Inc. to be electronically filed with the Clerk of the Court using CM/ECF, which will automatically send email notification of such filing to the following counsel of record:

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CERTIFICATE OF COMPLIANCE

I hereby certify that Pursuant to Rules 29(d) and 32(a)(7) of the Federal Rules of Appellate Procedure and of Federal Circuit Rule 32(b), the enclosed brief complies with the length limits set forth at Federal Rule of Appellate Procedure 29(d). The brief's type size and type face comply with Federal Rule of Appellate Procedure 32(a)(5) and (6). According to the word processing system used to prepare this brief (Microsoft Word 2010), the word count of the brief is 13,884 words not including the certificate of interest, corporate disclosure statement, table of contents, table of authorities, any addendum containing statutes, rules or regulations, and any certificates of counsel.

DATED: August 22, 2014

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